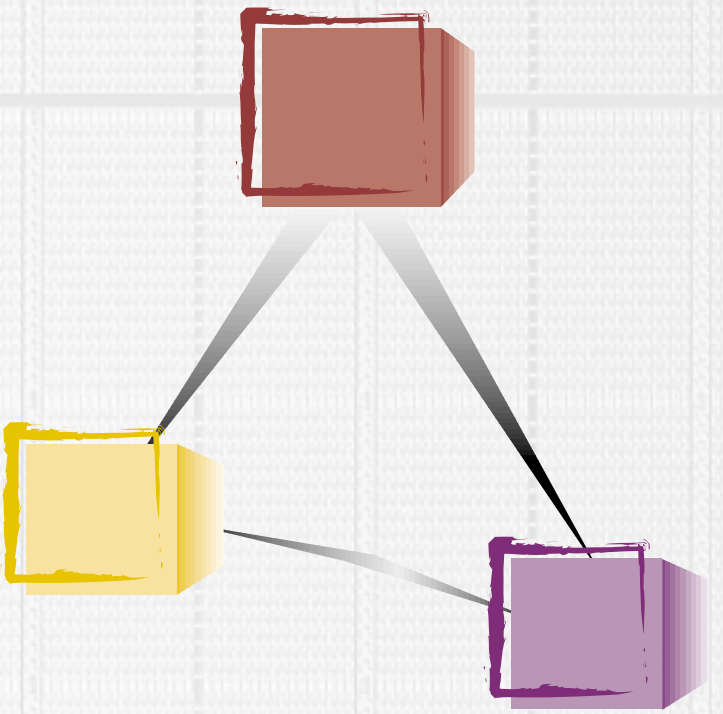
Actel's ProASIC Family

The Only ASIC Design Flow FPGA

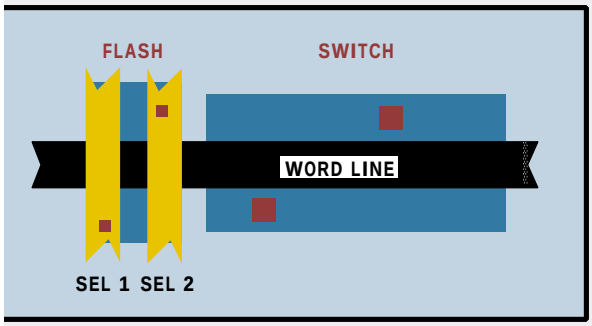
- *ASIC-like Design Flow*
  - *-Easy Timing Closure*
  - *-Familiar Design Tools*
- *Nonvolatile and Reprogrammable*
- *Low Power Consumption*
- *Flexible Embedded User Memory*
  - *-Built in FIFO control logic*
- *JTAG/IEEE 1149.1 Compliant*
- *High Performance Routing*
  - *-100% Automatic Place and Route at 100% utilization*
  - *-Fix Pins at >90% utilization*



Actel

The Flash Advantage

ProASIC Flash Switch



High Density

With densities ranging from 98,000 to 473,000 gates, 200MHz system performance, and up to 65k bits of embedded SRAM memory, Actel's ProASIC™ 500K family of programmable logic delivers high density programmable logic solutions. Using a .25µ standard CMOS/Flash process, ProASIC 500K devices combine high performance and low power with nonvolatility and reprogrammability. Combining industry standard ASIC or FPGA design methodologies and tools with easy IP re-use ProASIC 500K devices offer true reprogrammable system integration solutions.

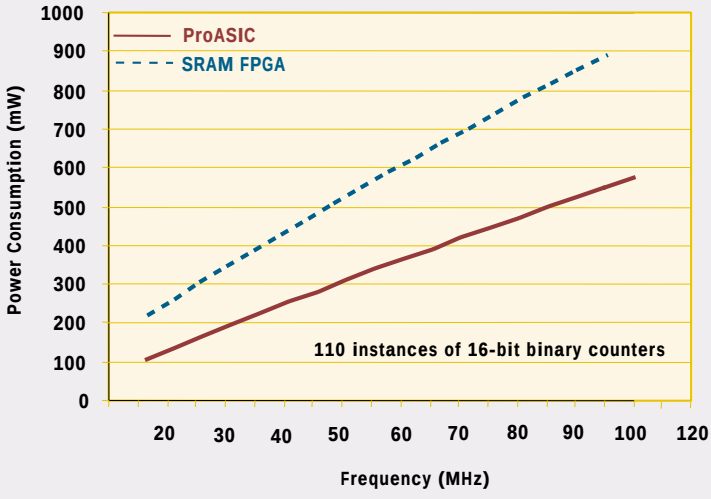
High Performance Architecture

Based on .25µ Flash technology that allows for performance enhancing architectural innovations, the small size of the Flash cell allows more programmable elements to be added into the routing, resulting in low resistance and low capacitance routing segments. These segments offer predictable performance, improved utilization, and greater routing efficiency. The very fine-grained logic drastically improves logic utilization and predictability. The ProASIC 500K devices also offer the ability to fix pins at greater than 90% logic utilization, resulting in easier system design and faster design iteration. ProASIC 500K devices are the optimal programmable solution to allow designers to easily meet performance goals.

Low Power

Along with the high performance comes low power consumption. With the inherent efficiency of the routing structure and the architecture of the logic cell, ProASIC 500K devices consume 1/2 the power compared to SRAM based FPGAs. This lower power consumption results in a significant reduction in overall system cost.

ProASIC Power Consumption



Nonvolatile and Reprogrammable

Because the ProASIC 500K devices are nonvolatile, they retain their configuration for a period exceeding the requirements of most sysyem lifetimes. This eliminates the cost of a boot PROM and the associated board space. Nonvolatile also means live on power up, so there is no period of nonfunctionality while configuration data is being downloaded from an external device. Additionally, ProASIC devices allow designers the flexibility to reprogram their devices if design changes are necessary. As they are live at power-up, ProASIC devices may implement the logic to control the power-up sequencing of other parts on the board.

Design Security

With the increasing complexity and density of devices, design security is a growing concern. ProASIC 500K devices offer an unprecedented level of design security. Without a startup bitstream, there is no possibility of the device's configuration data being intercepted. The devices also contain a read-protect security mechanism that prevents the programming content from being read out of the device. This read-protect mechanism cannot be cleared unless the entire device is erased.

IP Re-Use

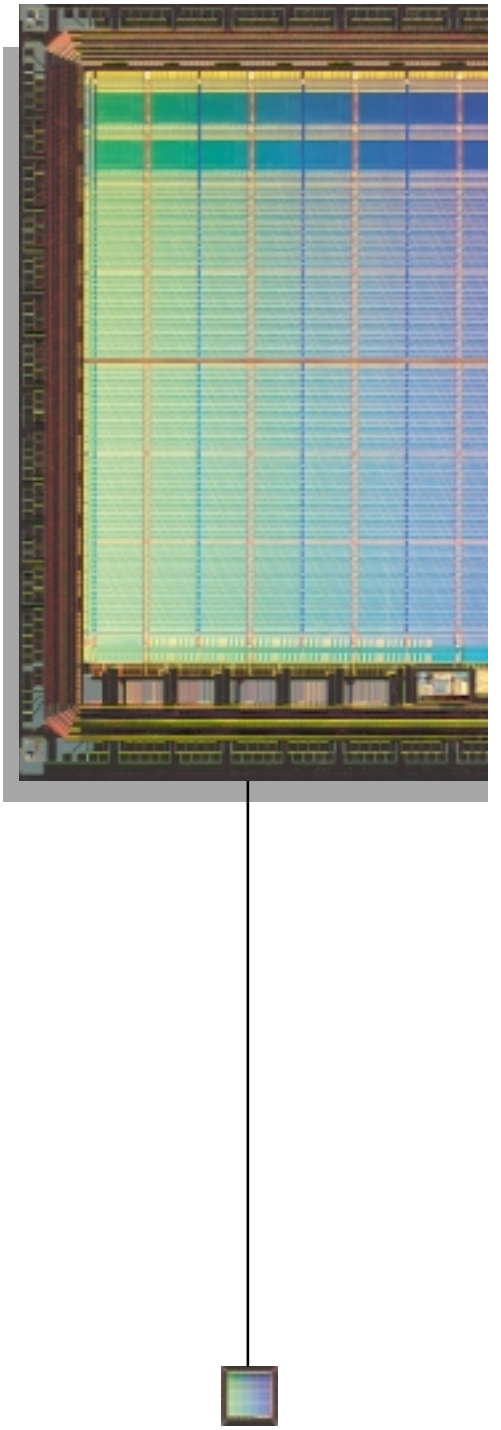
With increasing time-to-market pressures, designers do not have the luxury of developing every function from scratch. Design re-use is an important factor in meeting productivity goals. Due to the ProASIC 500K family's ASIC methodology and gate array-like architecture, bi-directional portability of functional blocks and commercially available IP between ASICs and ProASIC is easily achieved.

ASIC and FPGA Design Flows

ProASIC devices work equally well with ASIC and FPGA methodologies. Designers who work in an FPGA design flow can take advantage of the ease of use and fast run times they have come to expect. ASIC designers will appreciate the high degree of control and easy integration into their existing design environment.

Because of the architecture, ProASIC 500K devices can use the same VHDL and Verilog HDL descriptions that are targeted for gate arrays and standard cells, freeing the designer from the limitations imposed upon HDL by some FPGA architectures. Additionally, standard ASIC tools are supported, protecting the designers' investment in tools and training while streamlining the design environment. As a result, the design team can focus on getting the design to market faster.

Compact Flash switches configure the chip functionality, the associated routing and clocking, and the underlying logic cell that provides the programmable gates. Each switch consists of an NMOS transistor combined with a Flash memory cell and is controlled by a common floating gate, resulting in higher performance with lower power consumption.



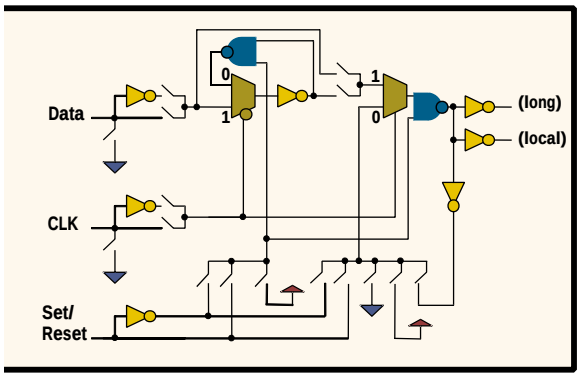
ProASIC A500K130 Die

Actual Size

ProASIC Architecture

A Technology of Innovation

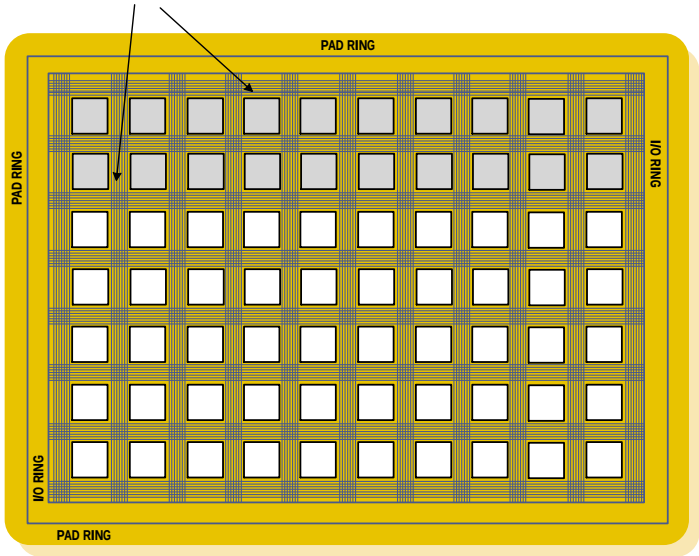
ProASIC Logic Tile



Logic Tiles

The small Flash switches makes it possible to utilize a fine-grained logic cell, resulting in better logic utilization. The basic logic tile consists of a programmable 3-input, 1-output cell. With the ability to program each input for signal inversion, the wasteful usage of cells as inverters is eliminated. Virtually any 3 input combinational logic function can be programmed, including flip-flops. This provides a great deal of flexibility, allowing a programming range from 100% combinatorial to 100% sequential. Through the programming of the local switch matrix, the cell is configured and combined with adjacent cells to form larger logic functions. Similar to a sea-of-gates gate array architecture, the basic logic tiles are stepped and repeated in the horizontal and vertical directions to create a programmable Sea-of-Tiles.™

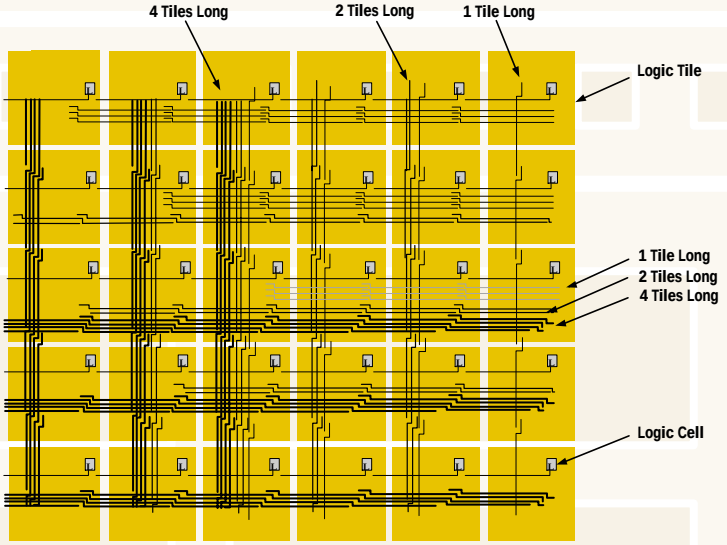
High Speed Bus Resource



Routing Resources

The interconnect routing resources are organized in four hierarchical levels, providing high performance with routing flexibility. This hierarchical routing structure provides optimal place and route solutions for varying design styles and application types. The four levels of routing networks are as follows:

- Ultra Fast Local resources are high speed dedicated lines that allow a direct connection from the output of every tile to I/O buffers, memory blocks, or the eight surrounding tiles.
- Efficient Long Line resources vary in length from 1, 2, or 4 tiles and provide routing for greater distance and higher fanout connections.
- High Speed Bus resources run vertically and horizontally across a chip. They are able to travel across the chip with minimal delay and can be used for busses, datapath functions, or very high fanout nets.
- High Performance Global networks are used to distribute clocks, resets, and other nets requiring high fanout with minimal delay and skew.



Ultra Fast Local and Efficient Long Line Resources

Embedded Two-Port SRAM

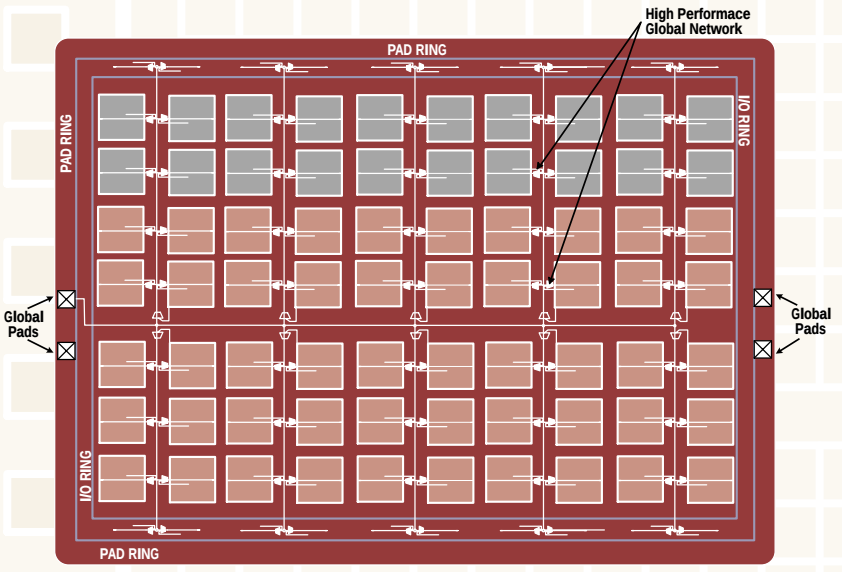
As chip densities increase, embedded and dedicated memories become essential. The ProASIC 500K devices provide up to 65k bits of embedded two-port SRAMs. Depending on the device, available memory ranges from 6 to 28 blocks that can support a variety of possible memory configurations. Each block contains a 256-word deep by 9-bit wide memory. With every block, there is the option to program it as an independent memory, or combine it with other blocks to form larger, more complex memories. Each memory block can be configured as synchronous or asynchronous, FIFO or SRAM. In addition, the memory blocks include hardwired decoder logic, I/O circuits, parity generation or detection circuits, FIFO flags generation logic, and timing and control circuits to minimize external logic gate count and complexity.

Programmable I/Os

The ProASIC 500K devices provide fully configurable I/Os for greater flexibility and performance. Each pad can be programmed as an input, an output, a three-state driver, or a bi-directional buffer.

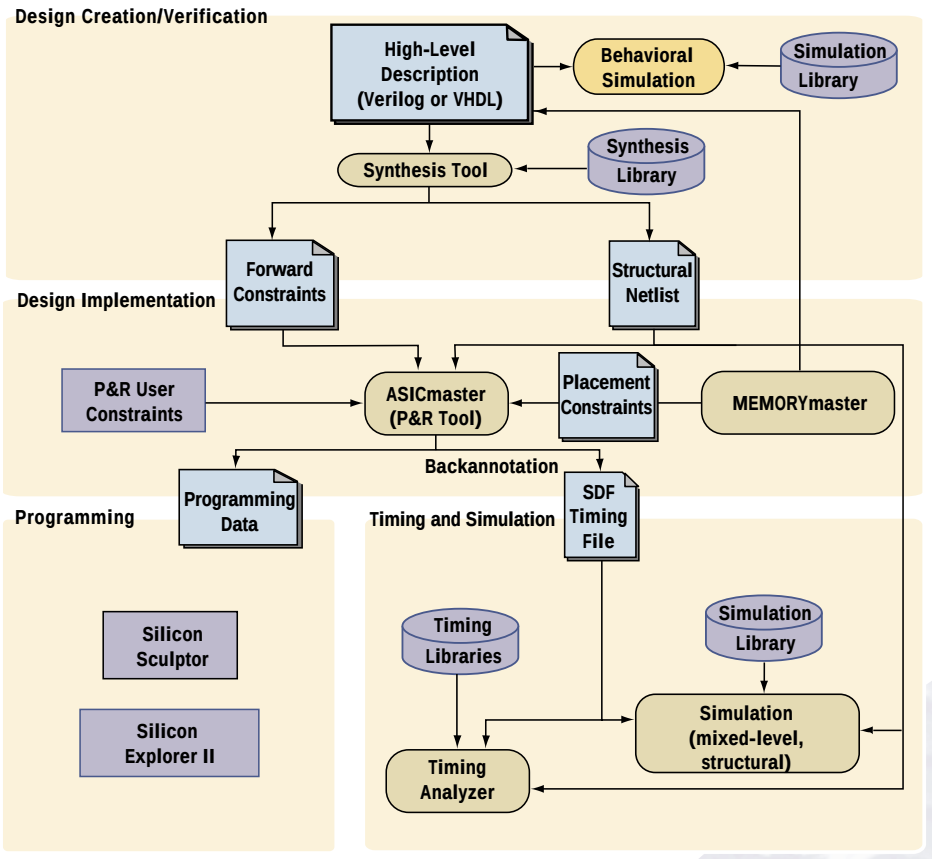
Additional programming options include pull-up resistors and selectable drive and slew rates that enable close matching to a wide range of bus interface conditions. The cells are programmed for LVCMOS or 3.3V PCI interface specifications. ProASIC 500K devices provide the capability to individually select each input/output device to interface with either 2.5V or 3.3V components.

High Performance Global Networks



Design Tools

Actel's ProASIC 500K devices are supported by ASICmaster™ and MEMORYmaster™ software, as well as third party CAE tools, offering designers an open design environment. ProASIC devices work equally well in ASIC and FPGA design environments, allowing designers to leverage their existing design tools.



ASICmaster

ASICmaster is an automatic place and route tool that runs on SunOS,® Solaris,® and HP-UX,® as well as on Windows® NT.™ ASICmaster accepts standard ASIC formatted netlists and performs timing-driven place and route. Incremental place and route is supported for ASIC-like ECO (Engineering Change Orders) capability. ASICmaster can be used as a push button tool, or as a fully user controlled process. ASICmaster also includes a power estimator and provides back annotated delay information for simulation or static timing analysis.

MEMORYmaster

MEMORYmaster is a tool that automatically generates RAMS and FIFOs according to configuration options set by the designer. The designer has the ability to select the depth and width, synchronous or asynchronous functionality of the ports, and usage of parity generation or check. If it is a synchronous read port, the designer can choose whether the output is pipelined or transparent. MEMORYmaster also generates a constraints file that contains placement information for created memory. Simulation models for all the configurations are provided in the design kit delivered on the ASICmaster CD.

Third Party Support

	Synthesis	Simulation	Static Timing
Synopsys	Design Compiler FPGA Compiler II FPGA Express	VSS	Prime Time
Cadence	BuildGates	Verilog-XL	
Exemplar	Leonardo Spectrum		
Model Techology		ModelSim	
Synplicity	Synplify		
VeriBest		VB VHDL VB Verilog	

Silicon Sculptor

ProASIC 500K devices have in-system programming capabilities using Actel's Silicon Sculptor. To program a device, the configuration data is supplied through a standard JTAG interface. Silicon Sculptor is a concurrent programmer that allows multiple sites to operate independently and enables the concurrent programming of multiple devices, speeding high volume production programming. The upcoming Silicon Explorer II will also provide configuration support.

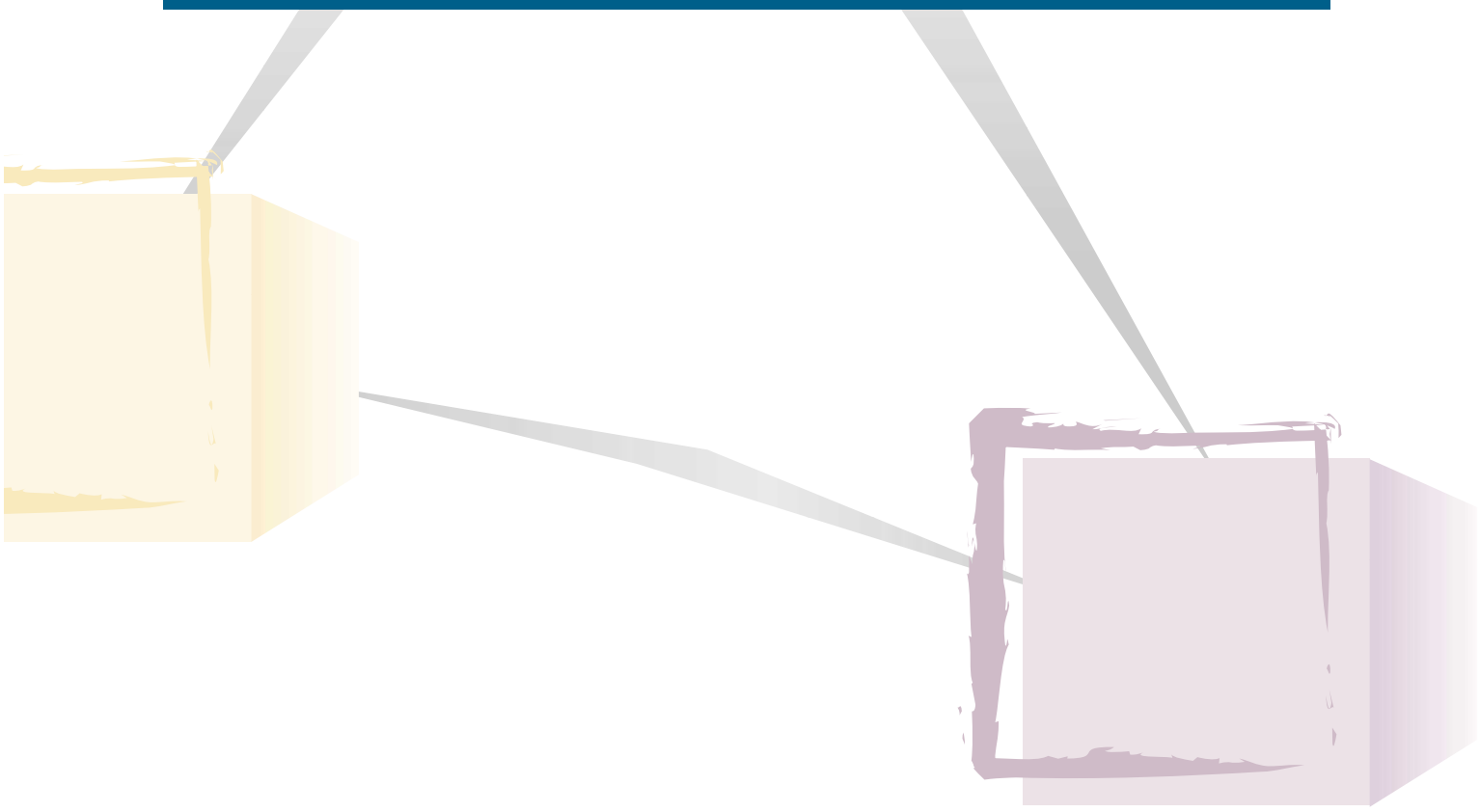
Protocol Design Services

The One Stop Design Solution

With a ten-year history of providing hardware and software services, Actel's Protocol Design Services team offers its customers design support at all stages of project development. With extensive knowledge of FPGA design and prototyping, services are delivered on time, within budget, and to the customers' specifications.

ProASIC 500K Family Selector Guide

	A500K050	A500K130	A500K180	A500K270
Maximum Gates	98,000	287,000	369,000	473,000
Typical Gates	43,000	105,000	150,000	215,000
Maximum Flip-Flops	5,376	12,800	18,432	26,880
Embedded RAM Bits	14k	46k	55k	65k
Embedded RAM Blocks (256x9)	6	20	24	28
Logic Tiles	5,376	12,800	18,432	26,880
User I/O	210	312	368	446
JTAG	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes



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