EE 4253/6253 Principles of VLSI Design — Class Policy and Syllabus — Fall 1998

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Textbooks:
- N.H.E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design, 2nd Ed.*, Addison-Wesley Pub., 1994.
- HSPICE manual set
- + class handouts

Grading:		
	(3) Exams	55%
	(1) Final	25%
	Labs & Homework	10%
	Project	10%
	Total	100%

Grade assignment is on a 10-point scale.

Lecture Classes will meet at the McCain Hall, room 353, from 8am-9:15am on Tuesdays & Thursdays. Class attendance is encouraged and strongly recommended.

Lecture Notes will be available on the Web in the form of postscript files at URL address **http://www.ece.msstate.edu/~blalock/vlsi/fall98** *if* not handed out in class. It is YOUR responsibility to print out the lecture notes weekly and bring them to class (once again, if not received in class). Do not use MPL or ECE printers! MSU provides Web printing resources for students at Butler Hall (for example).

One of the homework assignments will address engineering ethics and will require the preparation of a well written, formal in style, document. Information on the web located at URL address http://www.engr.washington.edu/epp/Pepl/Ethics will be helpful while doing this assignment.

VLSI Laboratory

Lab/Project policy: If you fail to hand in TWO or more labs you will be assigned an 'F' in the course regardless of test average. If you fail to hand in the Project you will also be assigned an 'F' in the course regardless of test average.

For on campus students, all labs will meet in Room 135 at Simrall. On campus VLSI Labs will meet at the following times:

Tuesdays	3:30-6:20pm
Wednesdays	3:00-5:50pm

Warning! Due to lab schedule conflicts with the CADD course, one lab section, probably the Wednesday section, will need to be moved to Friday (on campus students only).

All labs will involve probably approximately 1/2 hour of lecture before starting, so BE ON TIME! Unless otherwise noted, labs will be due at the beginning of your assigned lab period one week after the lab was handed out. All lab materials must be contained in an MSU lab folder.

Your assigned lab hours are the ONLY time you are guaranteed a workstation in Simrall 135. You will NOT be allowed to use a workstation during a normal period if you are not assigned that lab period. Outside of these lab hours, Simrall 135 workstations are available on a first-come, first-serve basis.

WARNING! If we find a workstation in Simrall 135 screen-looked by a VLSI student, 10 points will be deducted from that student's last VLSI test grade. We do NOT have enough workstations resources to allow screen-locking.

SYLLABUS

Course Topics and Order of Coverage

Week 1 (Aug25, Aug27):	Introduction to CMOS Circuits	Chpt. 1
Week 2 (Sept1, Sept3; Lab 1):	CMOS Transistor Theory	Chpt. 2
Week 3 (Sept8, Sept10; Lab 2):	CMOS Transistor Theory, CMOS Process Video	Chpt. 3
Week 4 (Sept15, Sept17; Lab 3):	CMOS Processes	Chpt. 2
Week 5 (Sept22, Sept24; **TEST#1**, Lab 4):	CMOS Layout	Chpt. 3
Week 6 (Sept29, Oct1; Lab 5):	CMOS Layout	Chpt. 3
Week 7 (Oct6, Oct8; Lab 6):	Delay Characterization	Chpt. 3
Week 8 (Oct13, Oct15; Lab 7):	Capacitance Characterization	Chpt. 4
Week 9 (Oct20, Oct22; Lab 8):	Standard Cell Methodology	
Week 10 (Oct27, Oct29; **TEST#2**, Lab 9):	Transient Analysis	
Week 11 (Nov3, Nov5; Lab 10):	Transient Analysis	
Week 12 (Nov10, Nov12; Lab Project Assignment):	Dynamic Logic	
Week 13 (Nov17, Nov19):	Dynamic Logic	
Week 14 (Nov24, **TEST#3**):		
Week 15 (Dec1, Dec3):	Dynamic Logic	
Week 16 (Dec8, Dec10; "Dead" days)	Review for Final, PROJECT DUE!!	

Final exam date: Thursday, December 17, 1998, 8:00-11:00am

Other important dates:

Sept4 Last day for registration, adding or dropping a course without a "W"
Oct5 Last day to drop a class with a "W" grade

Disclaimer:

The syllabus is subject to change! Updated versions will be available on the course's homepage.