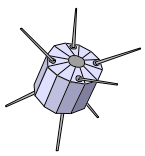
# TEMIC / MATRA MHS
# RADIATION TOLERANT SPARC PROCESSOR

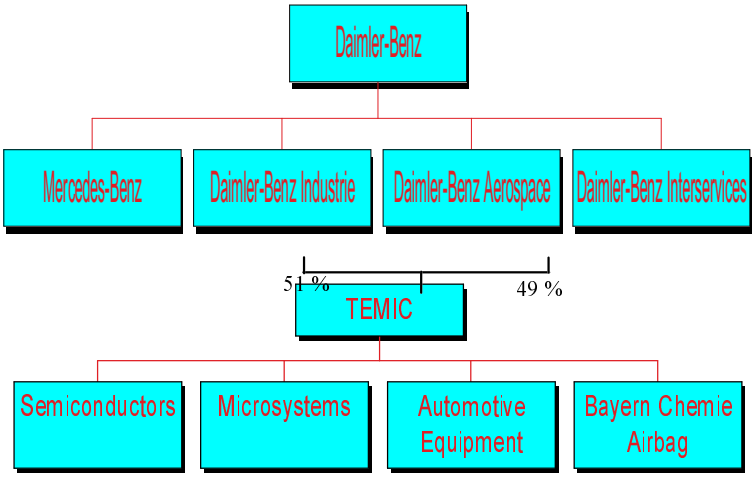
**by Dominique de SAINT ROMAN**

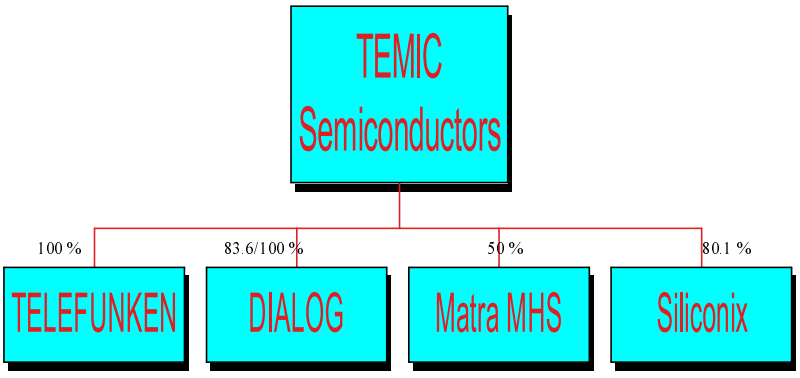
**ESA / ESTEC SPARC DAY**
**October 1, 96**

## AGENDA

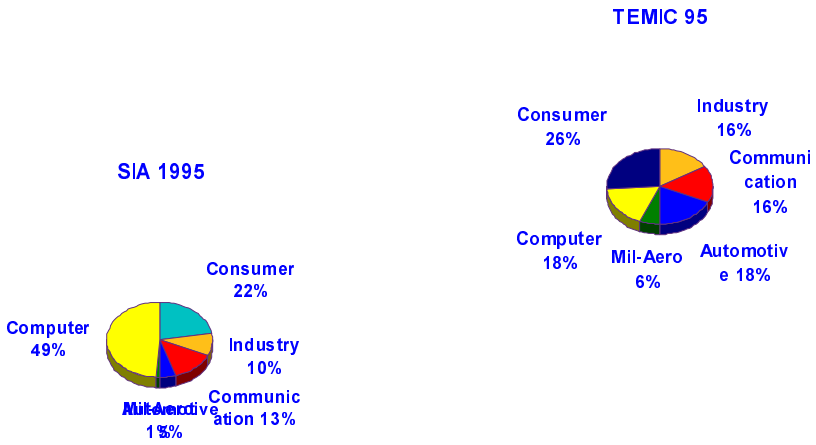
- TEMIC
- MATRA space strategy and product offering
- Radiation tolerant SPARC program
- SPARC status
- SPARC performances
- SPARC offering
- SPARC development support
- Forecast/conclusion




Daimler-Benz
Mercedes-Benz
Daimler-Benz Industrie
Daimler-Benz Aerospace
Daimler-Benz Interservices
51 %
49 %
TEMIC
Semiconductors
Microsystems
Automotive Equipment
Bayern Chemie Airbag

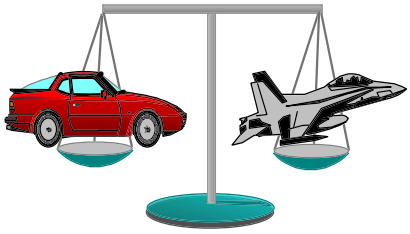

TEMIC Semiconductors
100 %
83.6/100 %
50 %
80.1 %
TELEFUNKEN
DIALOG
Matra MHS
Siliconix

## Revenue Structure by Market Segments

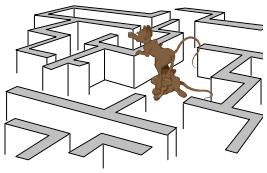



## TEMIC DUAL USE

- RT processes are only slight deviations from standards
- Non RT & RT products are mask compatible
- Non RT & RT products take advantage of volume based production:
  - ▼available in any packages to any quality grades
  - ▼better manufacturing & quality control
  - ▼broader innovation capability
  - ▼lower manufacturing cost
  - ▼better reproducibility
  - ▼better longevity



# TEMIC DUAL USE



- **TEMIC has been a pioneer, from company day one**
- **The only long term reliable route to keep servicing space**
- **The only route for space advanced technology availability**
- **The TEMIC brochure supports and emphasizes that strategy**
- **William PERRY supports it**
- **And everybody wants now to go that way !**

TEMIC
Semiconductors

# Space products offering

ASICs :

*Gate array* in CMOS 0.8µm : MCRT ---> 50K, 100 MHz
*Sea of gates* in CMOS 0.6µm : MG1RT ---> 480Kcells 250 MHz @ 5 V
*Sea of gates* in CMOS 0,5µm : MG2RT ---> 500Kcells 250 MHz @ 3V ( Q497 )
*Sea of gates* in CMOS 0,5µm : MG2RT ---> 500Kcells 350 MHz @ 5V ( Q497 )
*Full Custom* in CMOS RT 0,8 to 0,5 µm
in CMOS RT + 0,6 µm ( Q197 )
in BICMOSRT 0,8 µm
in DMILL 0,8 µm ( Q297 )

ASSPs :

16 and 32 bit EDACs, Discrete Cosine Transform
High Speed Data Link Tx/Rx ( Q496 )
Viterbi, Reed Solomon ( Q197 )

ULC :

FPGA conversions

TEMIC

MEMORIES

VLP SRAMs :
16K, 64K, 256K, 1Mbits ( Q4 96 )
VLP FIFOs :
512 to 16K x9, 15ns, 200µA
VLP DPRs :
1Kx8 MS to 8Kx16 MS, 20ns, 200µ

MICROS

Fast 8 bit µC :
80C32 30MHz
32 bit RISC :
SPARC µP chipset: IU, FPU, MEC
SPARClet µC ( Q497 )
32 bit floating point DSP :
TSC21020E, 20 MIPs ( Q297 )

Die
Hermetic
RAD-PACK TM ( Q1 97 )

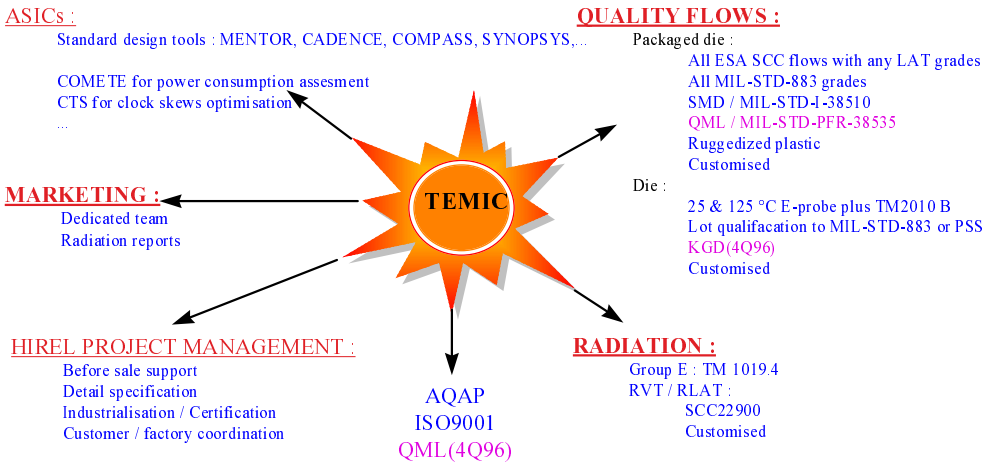
A Company of Daimler-Benz

RAD-PACK is a SEI trademark

Aerospace & Defense

TEMIC Semiconductors

## Services offering

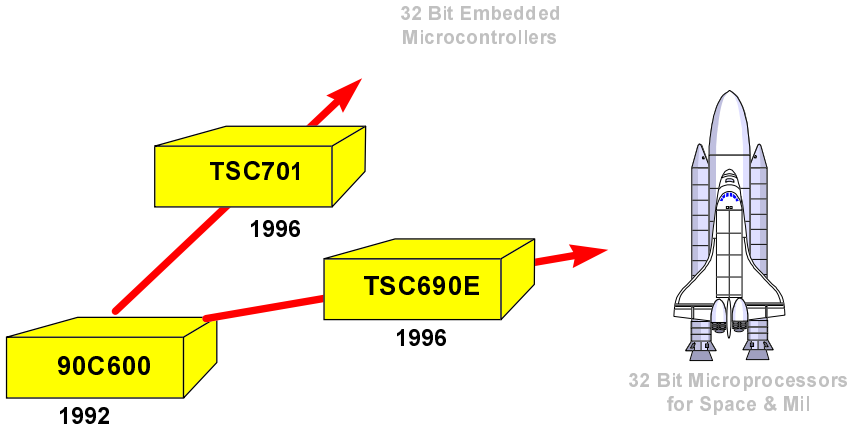



A Company of Daimler-Benz

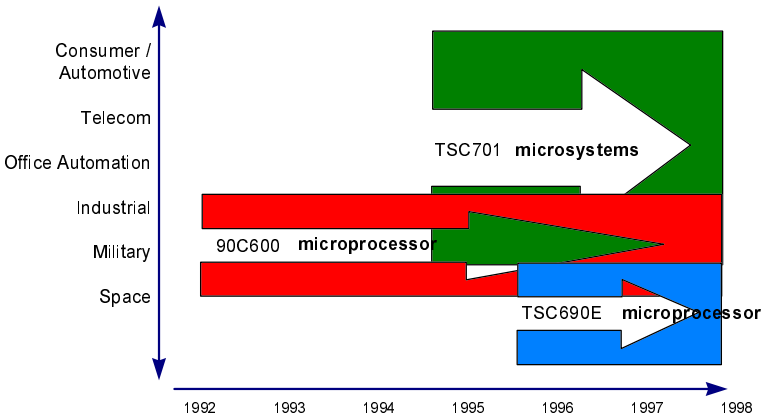
## Historical Context

- ESA intended to launch a new Microprocessor development programme
- Need of a space 32 bits Microprocessor from a European supplier
- Only MIL31750 was available on SOS technology, and wasn't powerful enough
- MHS was a good candidate with the SPARC architecture, and also thanks to its advanc radiation tolerant technology .
- Then, the SES, Matra Marconi Space and MHS consortium was selected to design a 32 b Computer named ERC 32 .

## 32 BIT SPARC PRODUCT LINES

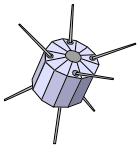



## MHS SPARC program



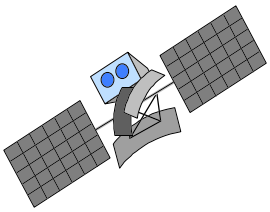
## TSC690E status

- Respective chips revision C, B and A are validated on DMS-R (beta site)
- Available :
  - ▼691E(IU), 692E(FP) and 693E(MEC) VHDL models
  - ▼respective chips revision are C, B and A
- Specifications :
  - ▼rev G, dated 10/09/96 for 691E and 692E
  - ▼rev B, dated 23/04/96 for 693E.
- Order entry open for C, B and A chips
- Irradiation completed :
  - ▼total dose at DCAN (France)
  - •SEU and latchup at Brookhaven Labs (USA)



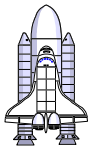
## TSC690E features

- Full functional compatibility with former 90C601 (IU) & 90C602 (FP)
- 100% compatible with SPARC V7
- Concurrent Error Detection
- Testability :
  - ▼Off-line testing with, at least, 95% fault coverage
- System self test after Power-On Reset covering 90% of the core
- Performance :
  - ▼10 Mips / 2 Mflops (SP) @ 14 MHz
- Power consumption :
  - ▼lower than 5 W (ERC32) @ 10 Mips
- Operating conditions :
  - ▼temperature range : -55°C to +125°C
  - ▼voltage range : 4.5V to 5.5V



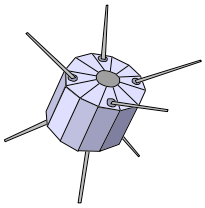
## TSC690E radiation features

- Total dose radiation (Gamma) :
  - ▼base line better than 50 Krads (Si)
  - ▼dual use process approach allowing non RT & RT versions
- SEU LET Threshold better than 15 MeV / cm2
- Latch up free (better than 100MeV)
- and over 97% of all SEU induced faults are detected and trapped



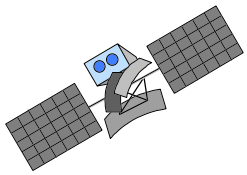
## Fault tolerant & test mechanisms

- Parity checking for all latches with generation of hardware error traps
- Parity checking for address, data & control busses
- Possibility to disable bus parity checking (internal still working)
- Master / checker operation for 691E and 692E
- Interleaving of register file bits for better SEU detection
- IEEE standard test access port
- Internal scan path
- Halt mode
- Program flow control (691E only)
- Operating & stand by power consumption reduction
- Process & design improvements for SEU & total dose
- Manufactured on space hardened 0.8 µm CMOS process



## TSC691E features

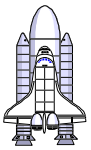
- Full software compatibility with 90C601
- 8 windows register files
- FPU interface allows concurrent execution of FP instructions
- User / supervisor modes for multitasking
- Fault tolerant & test mechanisms improvements
- Packaged into an MQFPF256(as TSC693E)



## TSC691E diagram

## TSC692E features

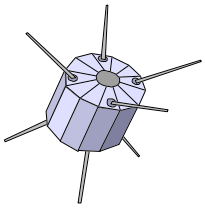
- Compatibility with 90C602 instructions set
- Full compliance with ANSI/ IEEE 754 for binary FP arithmetic
- 90C602E never generates unfinished FP operation exception
- Supports single and double precision FP operations
- Tightly coupled IU interface
- 64 bit ALU and multiplier/divide/square root
- 16 64-bit or 32 32-bit registers in 3 port FP register file
- Fault tolerant & test mechanism improvements
- Packaged into an MQFPL160



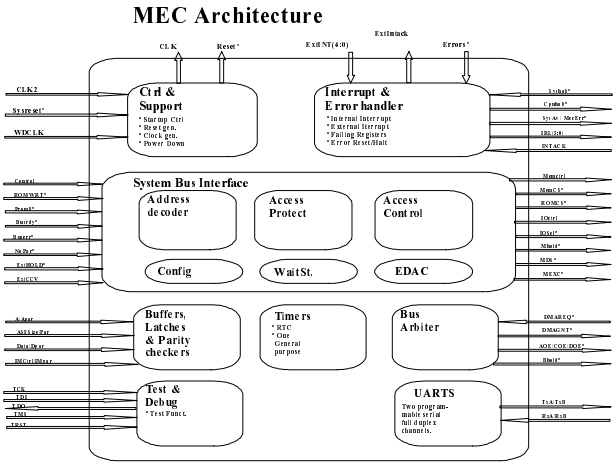
## TSC692E diagram

# TSC693E features

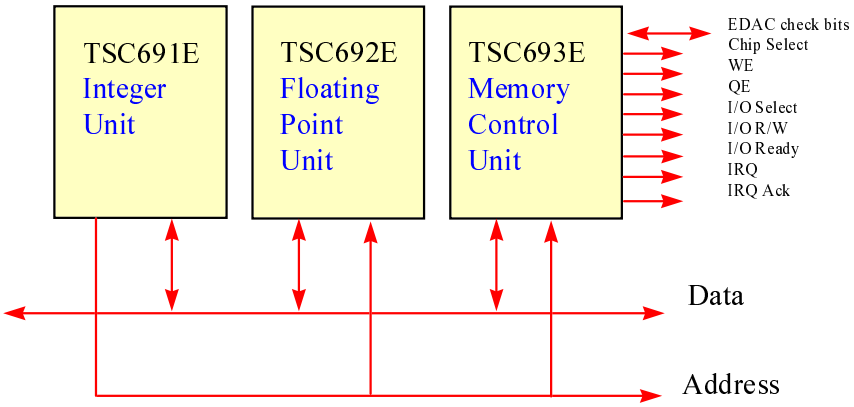
- Address decoding & memory interface
- Wait state generation
- Interrupt controller
- 32-bit SEC/DED
- Two 32-bit timers
- Two UARTs
- Boot PROM interface
- DMA interface
- Error manager
- Watchdog
- Packaged into MQFPF256 (as TSC691E)



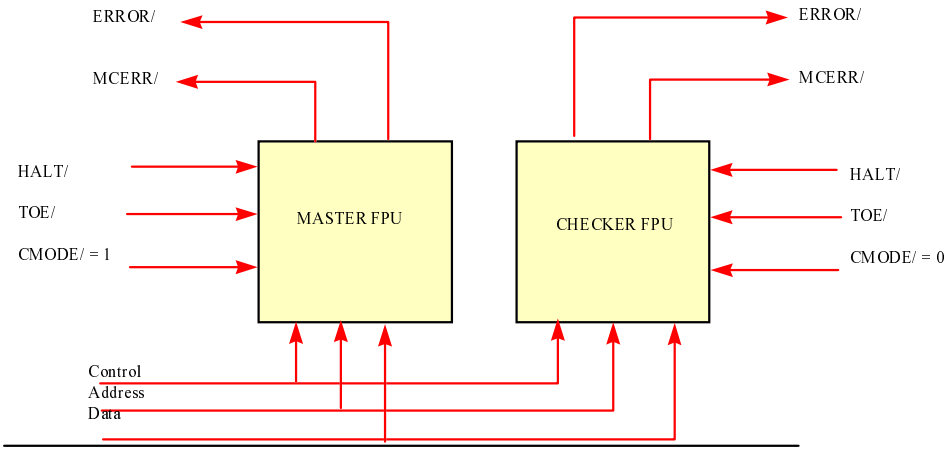
# TSC693E diagram



## Exemple of chips association

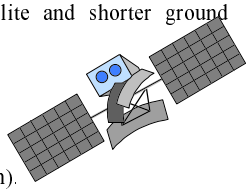



## Master/Checker Operation



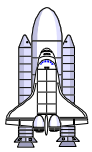
## Targetted applications

- TSC691E/TSC692E/TSC693E applications :
  - ▼ HARD REAL TIME
    - Attitude Orbit Control Satellite (AOCS),Control Navigation Guidance for Launcher,Spacecraft, Satellite platforms
  - ▼ DATA PROCESSING
    - Mission computer, Data management/storage for larger satellite and shorter ground communications
    - Dedicated payload processing
    - Worstations for Space stations
  - ▼ DATA HANDLING
    - Communication management
    - Data compression ( image : earth observation, datacommunication).
  - ▼ SMALL SATELLITE MULTIPLE COMPUTER USAGE
  - ▼ EMBEDDED APPLICATION



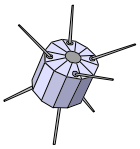
## Strengths

- Strong ESA recommandation for future developments
- Baseline for a majority of the new European Computer developments
- SPARC software available and standard ADA language can be used
- Many hardwares available for prototype development
- Capability to evoluate towards Sparclet core for the new generation
- Well known RISC instructions set
- Well adapted for multi application development
- TEMIC silicon for good traceability



## ERC32 quality flows

- So far, only delivered as packaged die, as follows :
  - a -E flow, which stands for engineering, which TEMIC will have available from the shelves, most of the time,
  - a -2 flow, which are parts packaged according MHS mil flow, with a mil temp range operating garantee, build on orders,
  - a P883 flow, which stands for MIL-STD-883 level B plus PIND test (TM2020 condition A), build on orders,
  - a SB flow, which stands for SCC9000 level B, build on orders.



## ERC32 software development tools : compilers & kernels

| PRODUCTS | COMPANY | AVAILABILITY | PRICE |
|---|---|---|---|
| ALSYS ADA | TSP / Alsys UK | Beta now | |
| VxWORKS C/C++ | Wind River France | Available | |
| GNU C/C++ | Public domain | Available | Free |
| RTEMS C/C++ RT kernel | OAR US | Available | Free |
| Rational ADA | Rational France | Available | |

## ERC32 software development tools : simulators, debugger, analysis

| PRODUCTS | COMPANY | AVAILABILITY | PRICE |
|---|---|---|---|
| **ERC32SIM (ERC32 simulator)** | SPACEBEL Belgium | Available | ? |
| **SIS (ERC32 simulator)** | ESTEC | Available | **Free** |
| **GDB & DDD (debugger and graphic user interface)** | Public domain | Available | **Free** |
| **Execution analysis tools** | SPACEBEL Belgium | ? | **?** |

## ERC32 software development tools : hardwares

| PRODUCTS | COMPANY | AVAILABILITY |
|---|---|---|
| **VME Common Processor Board** | MMS France | Available + specification |
| **DEM32 ERC32 evaluation board** | SES | Available + specification |
| **AVECS VME board** | DASA | ? |
| **SPARC RT VME single board computer** | THARSYS France | ? |