Axcelerator Family FPGAs Errata

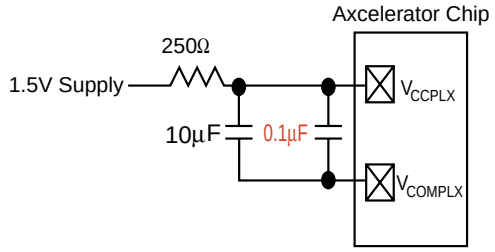
Some errors were found in the Axcelerator data sheet. The corrections, noted below, will be incorporated into a revised version of the data sheet. The changes in the graphics are indicated in red font. Within the body, corrections are in bold.

Page 1

1. Under Leading-Edge Performance, the fourth bullet should read **700**Mb/s LVDS Capable I/Os.

Page 16

1. In the figure, the value for the capacitor on the right is incorrectly shown as 100µF. The correct value is **0.1µF**.



Page 68, Axcelerator Clock Management System

1. In this section, it is not clear that REFP can be configured as single-ended or voltage-referenced standards. In the 2nd column, paragraph three, the last sentence should read: "In particular, the REFP pad can be configured as a differential pair, single-ended or voltage-referenced standard. The REFN pad can only be used as a differential pair with REFP."
2. The capacitors' values are incorrectly stated as 10pF and 100-250pf. The correct values are 0.1µF and 10µF. In the 2nd column, paragraph two, the fourth sentence should read: "Furthermore, **0.1µF and 10µF** decoupling capacitors should be connected across V_{CCPLL} and $V_{CompPLL}$ pins."
3. The resistor value is incorrectly stated as 100-200Ω. The correct value is 250Ω. In the 2nd column, paragraph two the third sentence should read: "The V_{CCPLL} pin should be connected to a 1.5V power supply through a **250Ω** resistor."
4. Figure 33 incorrectly shows the capacitors' values as 10pF and 100-250pf. The values should be **10µF and 0.1µF**. See corrected figure below.
5. Figure 33 incorrectly shows the resistor value as 100-200Ω. The correct value is **250Ω**. See corrected figure below.

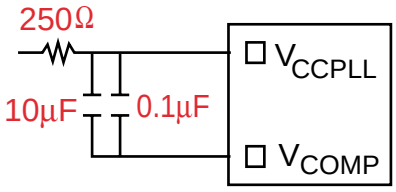


Figure 33 *PLL Electrical Interface*

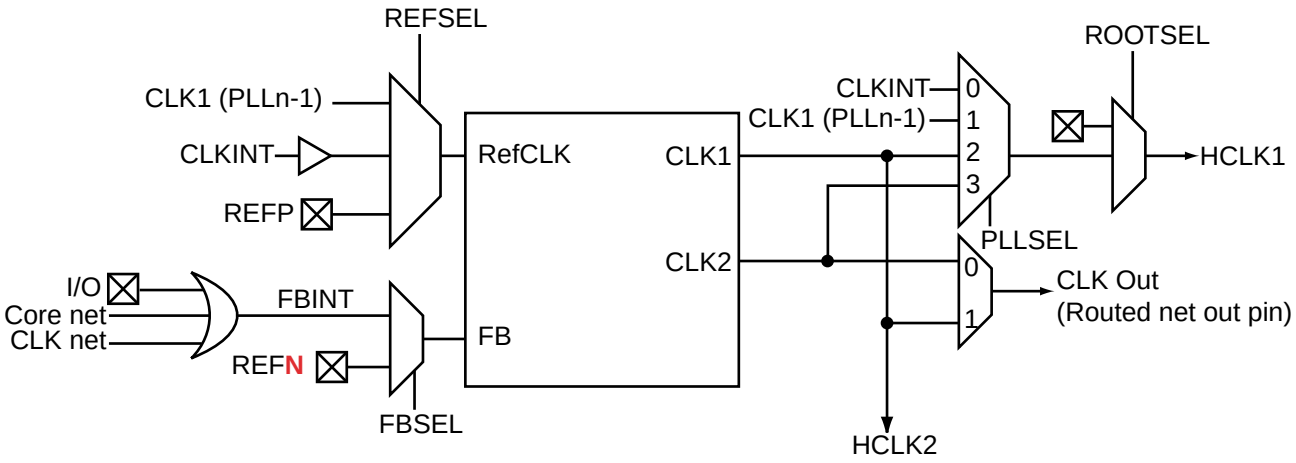
Page 70

1. In the PLL Signals table in the third body row the function of the PowerDown signal is incorrectly stated as When “high” powers down the PLL. The correct function is “When **‘low’** powers down the PLL.” Note that the table below is only a portion of the entire table.

PLL Signals

Signal Name	Type	Function
RefCLK	Input	Reference clock for PLL.
FB	Input	Feedback port for PLL.
PowerDown	Input	When **“low”** powers down the PLL.

2. In the interface block diagram one of the signals is shown incorrectly as REFD. It should be **REFN**.

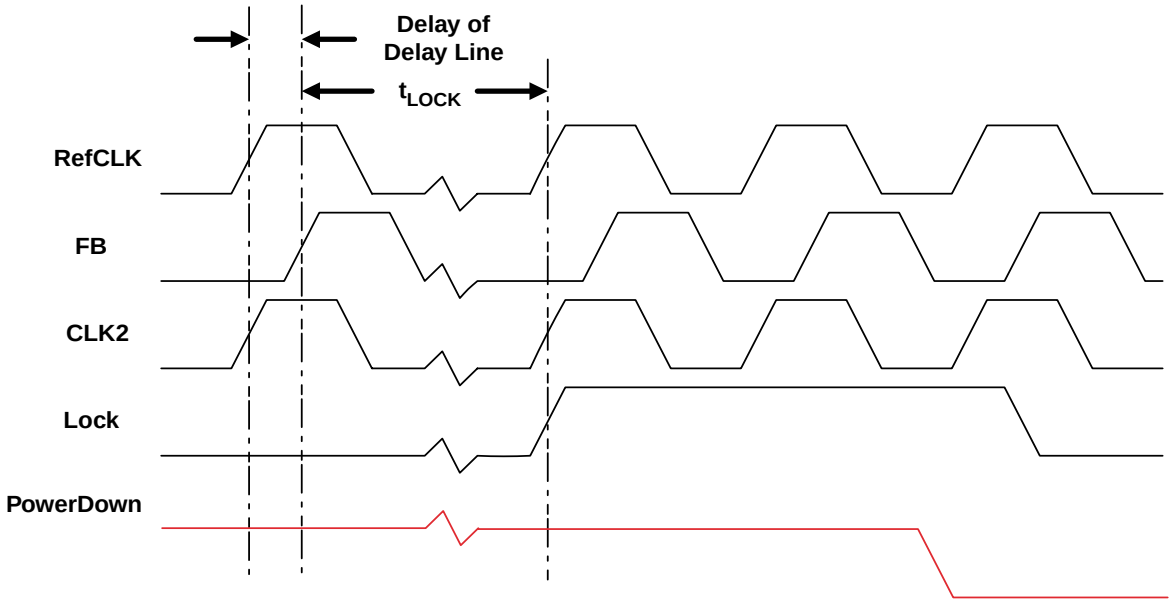


Page 71

1. Under “Power Down” it incorrectly states that the PLL includes an active-high power down signal. It sentence should read: “The PLL also includes an **active-low** power down signal and consumes very little standby current in this mode.”

Page 75

2. In the timing waveform diagram, the PowerDown signal is drawn incorrectly. The figure below shows how it should appear.



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