# Board Level Considerations for Actel FPGAs

## Introduction

Simulating and debugging individual components is the first step towards verifying a system design. In some cases, the devices no longer behave as expected after they are integrated. Many factors, such as power, airflow, and transmission lines can introduce undesirable results in a system and ultimately impair system performance. This application note will explain how many of these factors should be treated when integrating Actel field programmable gate arrays (FPGAs) in board-level designs.

## Power Up

Actel FPGAs are nonvolatile and therefore require no external configuration circuitry on power up. However, at power up it does take a finite amount of time for the device to become stable and operate normally. For a $V_{CC}$ slew rate of ~30 ns/V, it takes approximately 250 µs for the device to become fully operational. Power up time varies with temperature, where cold is worst case. At power up, the state of all flip-flops is undefined. Refer to "A Power On Reset Circuit for Actel Devices" application note later in this section for more information.

## Operating Environment

Actel FPGAs must not be operated outside of the recommended operating conditions as described in the Absolute Maximum Ratings section of their data sheets. Exposure to maximum rated conditions for prolonged periods may result in irreparable damage to the device.

As can be seen in the timing derating section of the data sheets, variations in voltage, temperature, and process will affect device performance. You must take care to design systems so that the effects of these variables, from best to worst case, will not cause timing problems during interchip communications.

## Thermal Considerations

An often overlooked test case examines ambient temperature effects on FPGA performance. Actel Designer Series software reports timing as derated by thermal junction temperature. This is the temperature found at the junction of the die and the package casing. Additional derating must be applied for ambient to junction temperature effects (θja). The value for θja will vary from package to package. The units for θja are °C/W. This implies that the power dissipation must first be calculated to determine the value for θja. (Please refer to the Power Dissipation section of the Actel data sheets.) Once θja is calculated, this temperature should be added at the junction to case temperature (θjc). This is the temperature value to be used for the temperature derating portion of the timing analysis. Because θja is a function of ambient temperature, the use of a fan can decrease the θja value. This can be seen by observing the difference between the θja value in still air and at 300 ft./min., as shown in the Package Thermal Characteristic section of the data sheets.

## Ground Bounce and Switching Characteristics

Actel defines simultaneously switching outputs (SSO) as any outputs that transition in phase within a 10 ns window. The resultant ground bounce produced is a function of the number of outputs switching simultaneously and the capacitive loading of the outputs.

Table 1 shows example SSO limits for Actel FPGAs at 50pF for ACT 1, ACT 2, and 1200XL families. Measuring techinques and SS0 limits for additional families and capacitive loads are defined in "Simultaneously Switching Output Limits for Actel FPGAs" application note later in this section.

***Table 1*** • *Example SSO Limits for Actel FPGAs*

| Device | Package | Maximum Recommended SSOs (50 pF load) |
|---|---|---|
| A1010A/A1020A | 44 PLCC | 16 |
| A1010A/A1020A | 68 PLCC | 24 |
| A1020A | 84 PLCC | 32 |
| A1010A/A1020A | 84 PGA | 32 |
| A1010A/A1020A | 100 PQFP | 32 |
| A1280/A1280XL | PG176, PQ160 | 64 |
| A1240/A1240XL | PG132, PQ144 | 48 |
| A1240/A1240XL/ A1225/A1225XL | 84 PLCC | 32 |
| A1225/A1225XL | 100 PGA, PQFP | 32 |

Exceeding the recommended limits results in a larger ground bounce. However, the width of the ground bounce pulse

prevents it from being recognized by most discrete digital receivers. Refer to the specifications of the external receivers for verification.[1]

Should you have the need to switch more signals than recommended, the SSOs should be distributed evenly around the device. This will reduce the amount of mutual inductance produced between adjacent I/Os and thus reduce the ground bounce.

Buffers may also be inserted in the path before the output buffer. This will reduce the possibility of adjacent signals switching within 10 ns of each other. The Actel Designer Series software should be used to verify the delays.

## Power and Ground Pins

Actel FPGAs are designed with ample power and ground pins on the device resulting in minimal ground bounce characteristics during I/O switching. A ground pin is provided for approximately every eight I/Os (please refer to package drawings found in this data book for further detail). Unused I/Os cannot be programmed to act as ground pins.

Table 2 describes the function of each of the power and ground pins found on the devices.

***Table 2 •*** *Power and Ground Pin Functions*

| | |
|---|---|
| $V_{CC}$ | Device operating power. |
| $V_{PP}$ | Device programming voltage. Should be tied to $V_{CC}$ during normal operation. |
| $V_{SV}$ | Super voltage supply. $V_{SV} = V_{PP} + 3$. $V_{SV}$ provides a precise lower limit on the voltage that is applied to a fuse during programming. During normal operation $V_{SV} = V_{CC}$. |
| $V_{KS}$ | $V_{KS}$ provides voltage supply for keepers (keepers maintain floating tracks at $V_{PP}/2$ during programming and prevent them from leaking down to GND). During programming, $V_{KS} = V_{PP}/2$. During normal operation, $V_{KS}$ = GND. |
| GND | Supplies GND to the array (all channels). |

## Slew Rate

ACT 1, ACT 2, 1200XL, and 3200DX device outputs operate at high slew rate only. Figures 1, 2, and 3 illustrate the slew rate characteristics for high slew rate outputs, both loaded and unloaded, for an A1280 PG176 device.

## Device I/O

The I/Os on each Actel FPGA are nonrestrictive. Any pin shown as an I/O in the pin description list can be assigned to be either input, output, bidirectional, or tri-state. ACT 2, 1200XL, and 3200DX FPGAs add latch capabilities to each of these options. Actel FPGAs do not incorporate any type of internal pullup on the I/Os. Inputs must not be left floating,

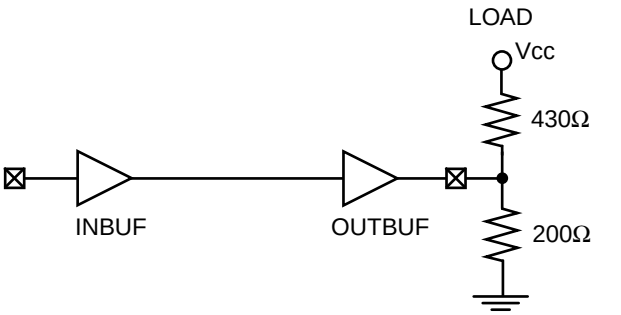



***Figure 1 •*** *A1280 Test Circuit*

since this may cause irreparable damage to the device. Any unused I/Os will be configured as active low outputs by the Designer Series System. The sink and source capabilities of individual outputs for ACT 1, ACT 2, 1200XL, and 3200DX FPGAs have been extrapolated from V-I curves and are shown in Table 3. The V-I curves for ACT 1 and ACT 2 devices are shown in Figures 4 through 9.

***Table 3 •*** *Worst-Case Sink and Source Current for Actel FPGAs*

| | ACT 1 | 1200XL and 3200DX |
|---|---|---|
| TTL | 8 mA | 10 mA |
| CMOS | 4 mA | 6 mA |

I/Os may be tied together externally to increase drive capability. The outputs must switch within 4 ns of each other, thus they should be placed as close to each other as possible. (Please refer to device die bonding diagrams for pad locations.) The switching times can be verified with the Actel Designer Series software.

## Decoupling Capacitors

Actel recommends the use of decoupling capacitors with all FPGA devices. We suggest a minimum of one capacitor per side, located next to power and ground. A 0.1 µF monolithic ceramic type is sufficient.

*References:*

1. David Shear, "EDN's Advanced CMOS Logic Ground-Bounce Tests," *EDN*, March 2, 1989, p. 88.

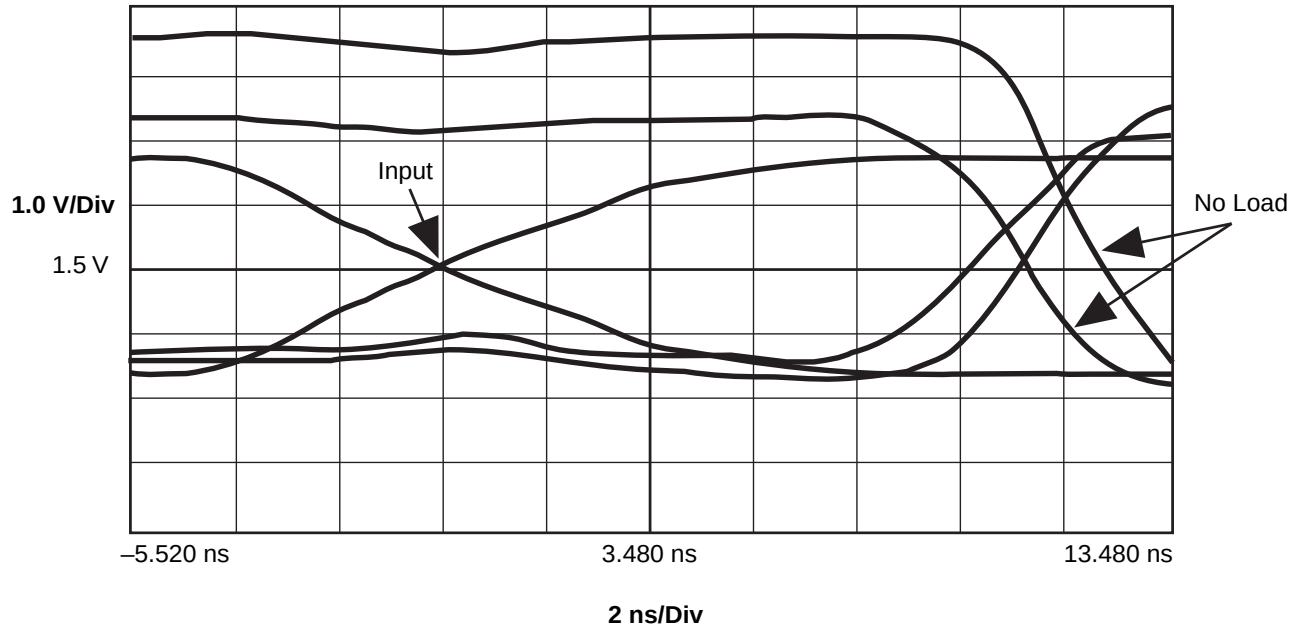
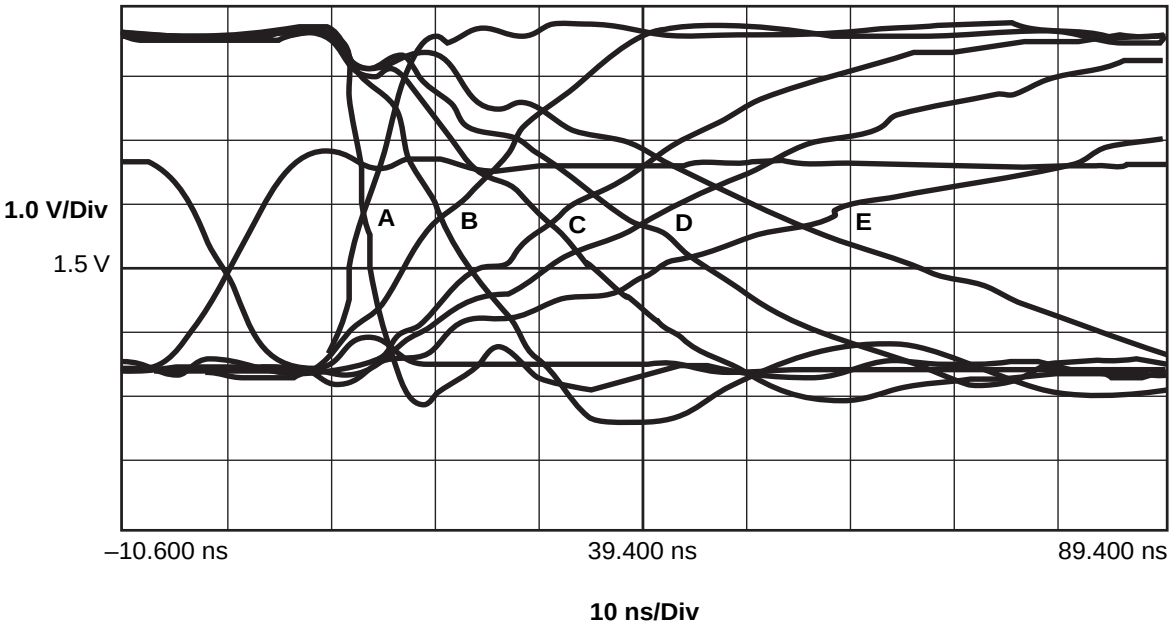
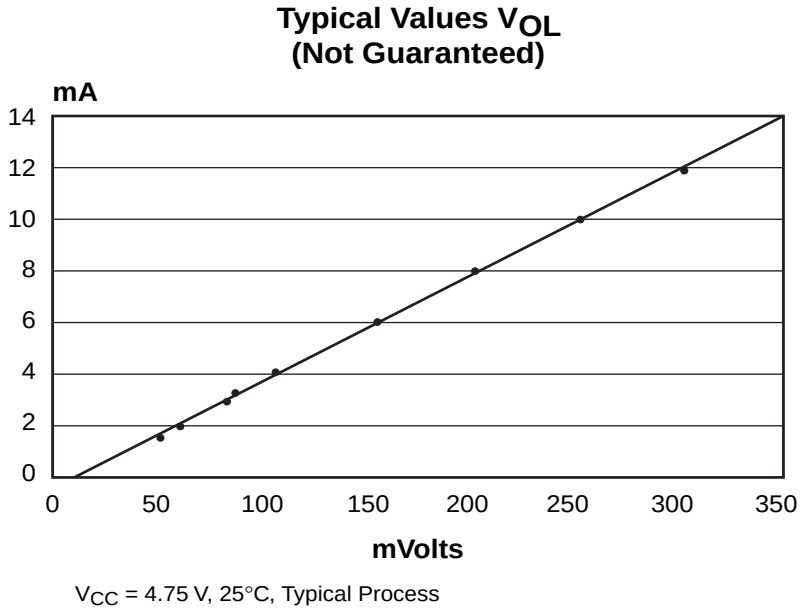



***Figure 2 •*** *A1280 No Load Versus Load—Fast Slew*




A = “No Capacitive Load” (~25 pF jig + 9 pF scope)
B = 82 pF
C = 200 pF
D = 300 pF
E = 560 pF

***Figure 3 •*** *A1280 Capacitive Loading Versus Slew*




$V_{CC}$ = 4.75 V, 25°C, Typical Process

***Figure 4 •*** *A1020A Typical Sink Current*

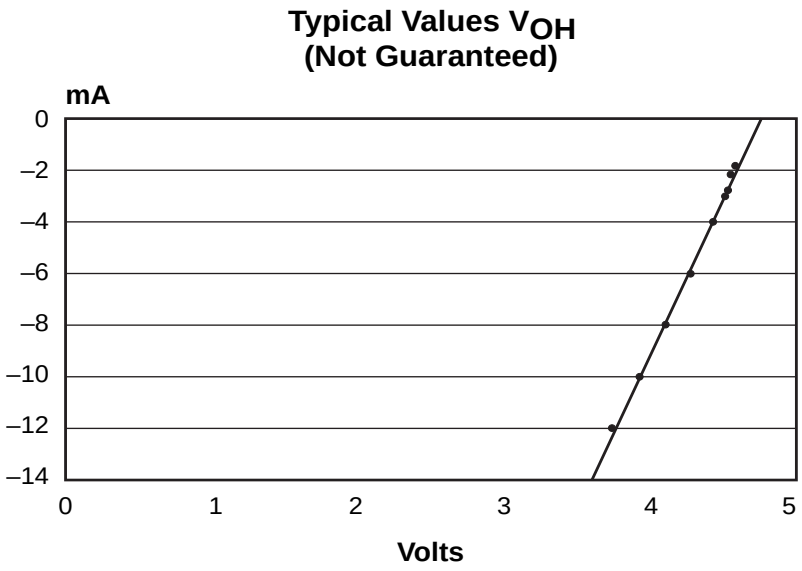



***Figure 5 •*** *A1020A Typical Source Current*

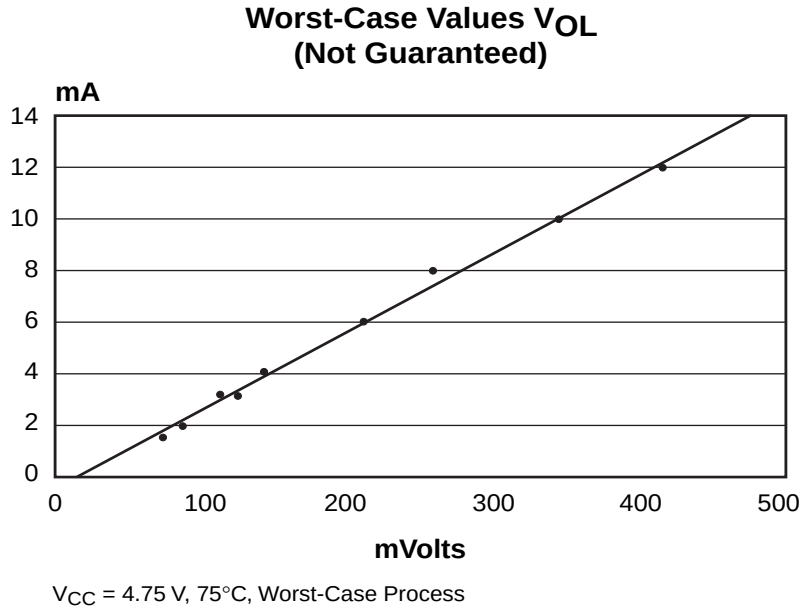



***Figure 6 •*** *A1020A Worst-Case Sink Current*

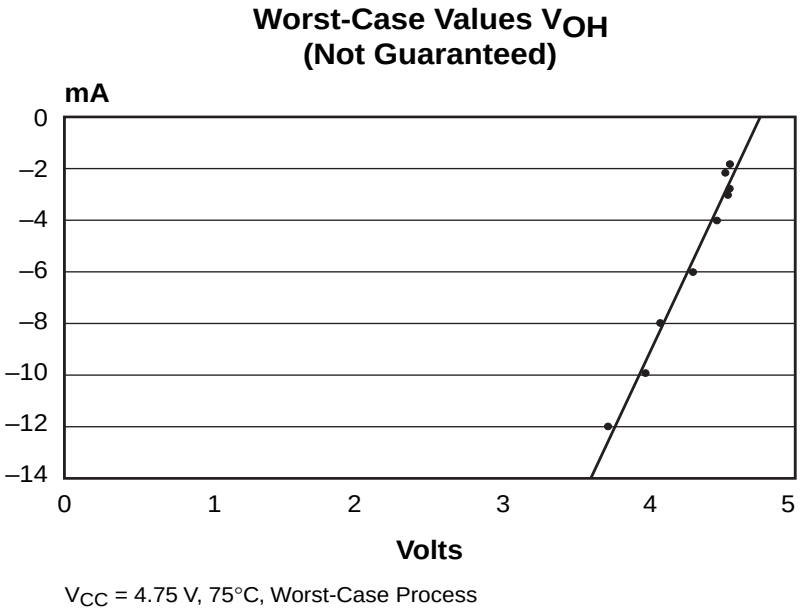



***Figure 7 •*** *A1020A Worst-Case Source Current*

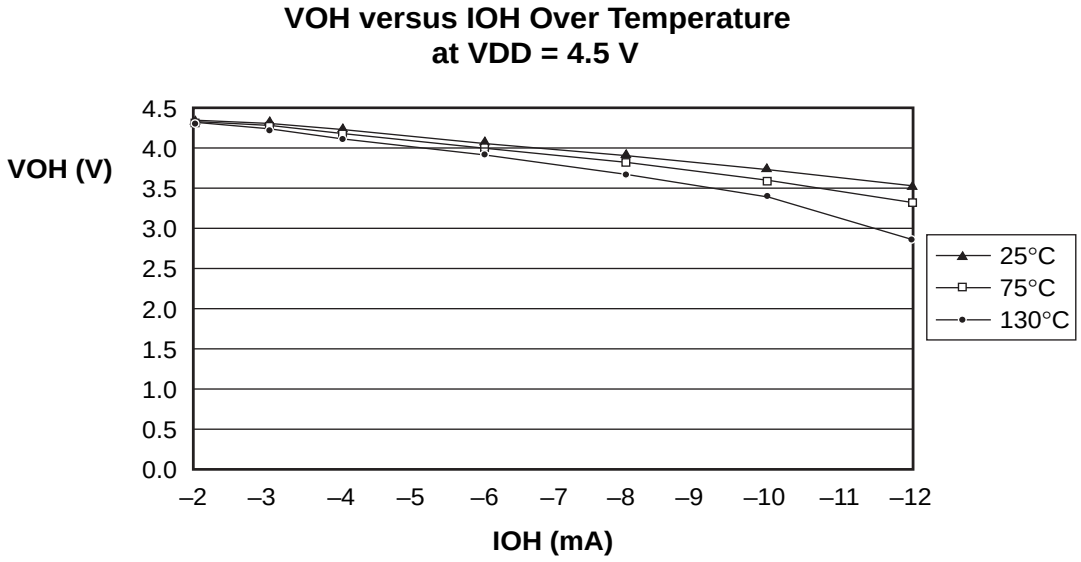



***Figure 8 •*** *A1280 Typical Source Current*

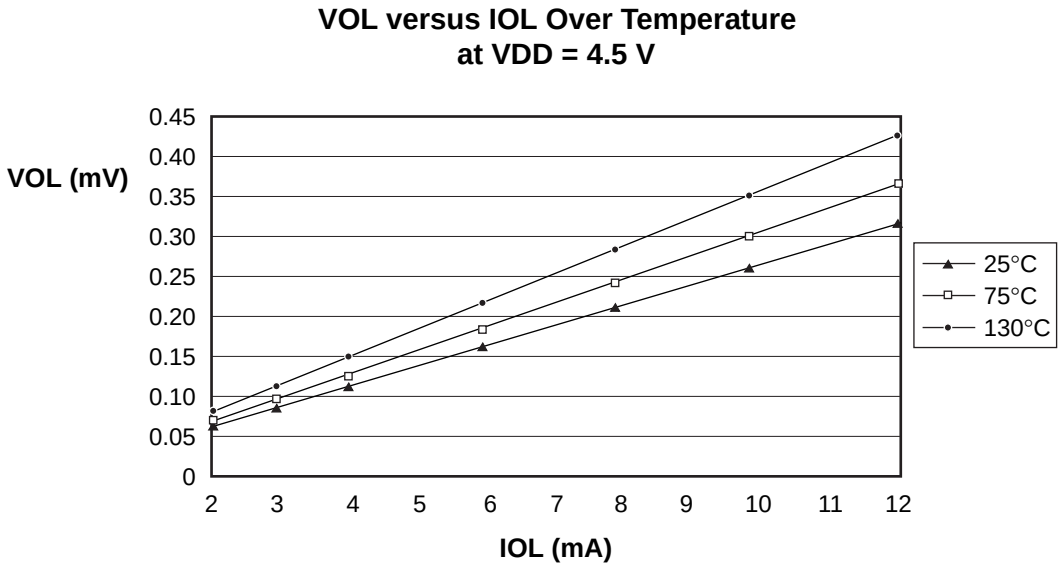



***Figure 9 •*** *A1280 Typical Sink Current*