Actel Designer R1-2003 FPGA Development Software Release Notes

This document describes the new features and enhancements of the Designer Series Development System R1-2003 release. It also contains information about discontinued features and known limitations.

Supported Platforms

Microsoft Windows - U.S. Version

- Windows 98, Second Edition (except APA750 and APA1000)
- Windows NT 4.0 with SP5 or SP6
- Windows 2000 with SP1 or SP2
- Windows XP

Sun Solaris

- Solaris 7
- Solaris 8

HP-UX

- HP-UX 11.0

Minimum System Requirements

Microsoft Windows 98/NT 4.0/2000/XP

- 300 MHz Pentium processor
- FAT32 or NTFS file system recommended
- 400 MB available on disk
- 128 MB System RAM
- CDROM drive
- HTML Browser
- 800x600 video resolution

Solaris 7, 8

- Sun Ultra processor
- 400 MB available on disk
- 256 MB System RAM
- HTML Browser

HP-UX 11.0

- HP processor
- 400 MB available on disk
- 256 MB System RAM
- HTML Browser

Installation and Licensing Instructions

Installation and Licensing Instructions are included with the software.

You must have a license that matches your software version in order to run Designer vR1-2003 (included w/ Libero v2.3). If you do not have a license to run software v.4.6 or above, your software will not work. Please update your license at http://register.actel.com/RegSerial.asp.

Device Support

ProASIC PLUS

The -F speed grade is now available in software for ProASIC PLUS devices. Please consult your Actel sales representative for availability of silicon devices.

Axcelerator

The package layout for the AX500-FG484 has changed.

- The following AX500-FG484 package pins are no longer bonded to I/O:

  C10, C11, C14, AB8, AB16

- The following AX500-FG484 package pins can now only be used as single

ended I/O:

AB7, AB17, C15

Please verify that your package layout conforms to these changes.

Note: Designer crashes if you open an old (pre-R1-2003) ADB file for the AX500-FG484 in R1-2003. To prevent this, export the EDN file and all the constraint files and create a new ADB file in Designer R1-2003.

New Features and Enhancements

Please see the user guides for details on each feature.

Timer

- Timer now supports skew analysis for ProASIC, ProASIC^{PLUS}, and Axcelerator Families
- The violation report now includes hold-time checking for ProASIC, ProASIC^{PLUS}, and Axcelerator Families
- Skew is now included in the analysis of the clock frequency
- The expanded path window now includes additional skew information for violation analysis
- Timer now grays out data that has been outdated by user constraints
- Constraints violations are now flagged on the summary tab
- In the summary and clock tab, you can now expand the path that is the source of the clock
- For designs with data feeding back in from a BIBUF I/O, Timer takes the feedback path into account for the reg-reg frequency calculation. This new feature may cause existing designs to show a different reg-reg frequency since this path was previously ignored. To obtain the reg-reg frequency without taking this path into account, either break the path at the enable pin of the BIBUF or set the path through the BIBUF as an exception.

APS

The APS programming software for the discontinued Activator 2 programmers is no longer installed.

Support for ProASIC and ProASIC^PLUS

The following modifications can be saved into the design database:

- Modification of a set of pins or a clock domain. These modifications result from removing a pin from the domain or adding a new pin into the domain.
- Modification of frequency values of a domain
- Modification of activity (annotation) of pins
- Deletion of an existing set of pins or a clock domain
- Creation of a new set of pins or a clock domain

Clock domains, Set-of-Pins, and annotated pins can now be included in the SmartPower text report.

Extended Layout Scripts

The R1-2003 release includes enhanced, extended layout scripts. These TCL scripts force the layout to run with an extended set of parameters and enable you to optimize for a specific clock. These scripts cause an increase in layout runtime in an attempt to improve performance and routability.

There are two scripts available, "iterate.tcl" and "sh_iterate.tcl".

Iterate.tcl

This script runs from the GUI and assumes that the design has been successfully compiled.

To execute the "iterate.tcl" script:

1. **From the File menu, select Execute Script**
2. **Select the "iterate.tcl" script.** Browse to the "scripts" directory within your Designer installation directory select "iterate.tcl". This script runs five iterations of the extended parameter layout.

   To change the number of iterations, add a "-n" and the number of iterations you wish the layout to attempt in the argument box (the maximum value for iterations is 26).

   To specify which a clock to optimize for, add a "-c" and the name of the clock you wish the layout to optimize.
3. **Click the Run button to run the script.**

Sh_iterate.tcl

This script is the command-line version of the iterate.tcl script and is recommended for UNIX users. This script also requires that the design has been successfully compiled.

Run this script from the acttclsh shell located in the "bin" directory (in your Actel designer installation directory). This script is located in the "script" directory of the Actel installation.

This script runs five iterations of the extended parameter layout. In order change the number of iterations, add a "-n" and the number of iterations you wish the layout to attempt. To specify which a clock to optimize for, add a "-c" and the name of the clock you wish the layout to optimize.

Netlist Viewer

Netlist Viewer now allows users to switch between pre-optimized and post-optimized design netlists for the Axcelerator family

Page navigation icons have been added to the toolbar to enable users to move across display pages in the Netlist Viewer

FlashLock

The FlashLock Permanent Lock feature is now enabled for the ProASIC^{PLUS} family.

Simulation

The ProASIC, ProASIC^{PLUS}, and Axcelerator RAM simulation models in Vital and Verilog have been updated to allow pre-loading of memory content for simulation. Please refer to the *Preloading of RAM Models in Simulation* application note.

Online Help

Designer now includes an error manager that links additional information to error messages. In addition:

- Online Help documentation has been revised and updated.
- HTML help has been added on the Windows Platforms.
- WebHelp has been added on UNIX platforms.

Resolved Issues

ACTgen

22759 - Using ACTgen for Axcelerator Designs

A problem with Axcelerator Fast Counter flags being reversed has been corrected.

22764 - Using ACTgen for ProASIC^{PLUS} Designs

ACTgen PLLs now function properly in simulation. An error in the output of ACTgen generated FIFO's has been corrected.

22480 - Using ACTgen for SX-A Designs

An issue with the almost full and almost empty flags being reversed resolved for SX-A FIFOs has been corrected.

Known Issues and Workarounds

A complete explanation of the Known Issues and Workarounds is available online at http://www.actel.com/custsup/updates/designer/R103rl.html

ACTgen

·22958 - Attempting to generate FIR-Filters with a width of 16 bits and 64 tabs may cause ACTgen to exit prematurely.

23018 - When specified from a GEN file, FIR filters always have the default value for DataMaxFo and clock frequency regardless of what was specified in the GEN file.

23280 - The accumulator for ProASIC^{PLUS} includes an ACLR pin which has an INOUT property even if no ACLR is selected for the accumulator.

23980 - For an async FIFO, if the empty flag goes low and RDB receives a rising edge (read-shift-register enabled), the read-shift-register advances by 1.

22845 - Register Files generated by ACTgen for SX-A have a port direction of INOUT for the Rclock pin.

22990 - Generate FIR filters for the SX-A family only from the “Basic Options” Tab.

16038 - Axcelerator CRC macros must have a width that is a power of 2. Attempting to generate a macro with a width that is not a power of 2 causes ACTgen to return an error, though it still generates a netlist. Do not use the generated netlist.

24055 - Axcelerator FIFOs created by ACTgen with flags must have Write Enable (WE) and Read Enable (RE). The "none" selection for the WE and RE signals are not legal for FIFOs with flags.

Compile

23481 - Compile fails if the net and the port in the netlist have the same name.

22420 - You must set register combining for Axcelerator before the compile stage.

24238 - Existing AX500-FG484 databases with pins that are no longer available in the device, (as described in the "Device Support" section), may cause the Designer software to abort prematurely.

Layout and Extended Layout

23509 - The extended layout script runs only in Timing Driven Mode for NON-ProASIC, -ProASIC^{PLUS}, and -Axcelerator families.

Reporting

23414 - Warning messages from SmartPower are only reported in the Output tab.

23326 - Error and warning messages do not appear in the error or warnings tabs for ProASIC and ProASIC^{PLUS} designs.

23492 - In the expanded Timer window, selecting the grid and clicking Edit -> Copy does not properly copy the entire grid.

FlashLock

23531 - While the FlashLock GUI allows for a security key of 66 characters for all ProASIC^{PLUS} devices, only the largest ProASIC^{PLUS} device allows 66 characters.

SmartPower

23869 - SmartPower GUI does not refresh properly.

23866 - SmartPower cannot accept a negative value for the ambient temperature.

24211 - For the ProASIC and ProASIC^{PLUS} devices, if any changes are made to the capacitance loading in PinEdit, you must close and re-open the design for the changes to be reflected in SmartPower.

Selecting the Domain tab after standard place-and-route executed from a script may cause SmartPower to exit prematurely on the HP-UX platform.

PinEdit

24460 - Do not assign a regular I/O macro to a PECL pad position.

Timer

Axcelerator

On "Register to Output" and "Input to Output" paths, Timer reports a delay that is over 1ns pessimistic.

23922 - In the expanded path frame for setup/hold checking, the network path delay for the source register is labeled "(longest)" and the network path delay for the sink is labeled "(shortest)". The label for the source register should be "(shortest)" and the label for the sink register should be "(longest)".

SX-A/SX-S

23378 - For the A54SX72A and RT54SX72S, the Timer shows three entries for each QCLKBUF used. Timer shows the internal nodes of the QCLK tree as clocks labeled "QCLKBUF_inst:D" and "QCLKBUF_inst:E".

Simulation

Model Technologies ModelSIM

23906 - Updates to the Vital libraries now require that the entity be compiled before the architecture.

24137 - The CLK2 output of the ProASIC^{PLUS} PLL does not produce an output in simulation. The CLK1 output of the PLL simulates normally. The simulation for both clock outputs simulate correctly in the Cadence NCSIM and the Model Technology ModelSIM.

PLLs for ProASIC PLUS

24462 - The GL (located adjacent to GLMX), GLMX and regular I/O pins may not drive the PLL in real silicon. You can prevent this problem if you do not have fixed pin assignments and use the GL pin adjacent to the PECL pad to drive the PLL.

Online Help

Error and Warning messages for the ProASIC and ProASIC PLUS families appear only in the output tab.