Mentor Graphics®

Interface Guide

R1-2002

UNIX® Environments

Actel

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Trademarks

Table of Contents

Introduction

This *Mentor Graphics Interface Guide* contains detailed information about using Mentor Graphics software to create designs for Actel devices. Refer to the *Designer User's Guide* for additional information about using the Designer software and the Mentor Graphics documentation for information about using Mentor Graphics tools.

Document Organization

The *Mentor Graphics Interface Guide* contains the following chapters:

Chapter 1 - Setup contains information about setting up Mentor Graphics tools to create Actel Designs.

Chapter 2 - Actel-Mentor Graphics Design Flow describes the design flow for creating Actel Designs using Mentor Graphics CAE tools.

Chapter 3 - Actel-Design Architect Design Considerations contains information for creating designs with Design Architect.

Chapter 4 - Simulation Using QuickSim II contains information about simulating Actel designs with QuickSim II.

Chapter 5 - Static-Timing Analysis Using QuickPath contains information about static timing analysis with QuickPath.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

This document assumes the following:

1. You have installed the Designer Series software.
2. You have installed the Mentor Graphics software.
3. You are familiar with UNIX operating system environments.
4. You are familiar with Actel FPGA architecture and Actel design software.

Document Conventions

This document uses the following conventions:

Information input by the user follows this format:

```
keyboard input
```

The contents of a file follows this format:

```
file contents
```

Messages displayed on the screen appear as follows:

```
Screen Message
```

This document uses the following variables:

- Actel FPGA family libraries are shown as <act_fam>. Substitute the desired Actel FPGA family ACT1, ACT2 (for ACT2 and 1200XL devices), ACT3, 3200DX, 40MX, 42MX, 54SX, 54SX-A, eX, and Express as needed. For example:

  ```
  edn2vhdl fam:<act_fam> <design_name>
  ```

- Compiled VHDL libraries are shown as <vhd_fam>. Substitute <vhd_fam> for the desired VHDL family ACT1, ACT2 (for ACT 2 and 1200XL devices), ACT3, A3200DX, A40MX, A42MX, A54SX, A54SX-A, eX, and Express as needed. The VHDL language requires that the library names begin with an alpha character.
-

Your Comments

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products, so you can get your work done quickly. We welcome your feedback about this guide and our online help. Please send your comments to **documentation@actel.com**.

Actel Manuals

Designer and Libero include printed and online manuals. The online manuals are in PDF format and available from Libero and Designer's Start Menus and on the CD-ROM. From the Start menu choose:

- Programs > Libero 2.2 > Libero 2.2 Documentation.
- Programs > Designer Series > R1-2002 Documentation

Also, the online manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the online manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

The Designer Series includes the following manuals, which provide additional information on designing Actel FPGAs:

Getting Started User's Guide. This manual contains information for using the Designer Series Development System software to create designs for, and program, Actel devices.

Designer User's Guide. This manual provides an introduction to the Designer series software as well as an explanation of its tools and features.

PinEdit User's Guide. This guide provides a detailed description of the PinEdit tool in Designer. It includes cross-platform explanations of all the PinEdit features.

ChipEdit User's Guide. This guide provides a detailed description of the ChipEdit tool in Designer. It includes a detailed explanation of the ChipEdit functionality.

Timer User's Guide. This guide provides a detailed description of the Timer tool in Designer. It includes a detailed explanation of the Timer functionality.

SmartPower User's Guide. This guide provides a detailed description of using the SmartPower tool to perform power analysis.

Netlist Viewer User's Guide. This guide provides a detailed description of the Netlist Viewer. Information on using the Netlist Viewer with Timer and ChipEdit to debug your netlist is provided.

A Guide to ACTgen Macros. This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

Silicon Expert User's Guide. This guide contains information to assist designers in the use of Actel's Silicon Expert tool.

Cadence® Interface Guide. This guide contains information to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

Synopsys®Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Innoveda® eProduct Designer Interface Guide (Windows). This guide contains information to assist designers in the design of Actel devices using eProduct Designer CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog Simulation Guide. This guide contains information to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Flash Pro User's Guide. This guide contains information about how to program Actel ProASIC and ProASIC PLUS devices using the Flash Pro software and device programmer.

Silicon Explorer II. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

ProASIC PLUS Macro Library Guide. This guide provides descriptions of Actel library elements for Actel ProASIC and ProASIC PLUS device families. Symbols, truth tables, and tile usage are included for all macros.

Online Help

The Designer Series software comes with online help. Online help specific to each software tool is available in Libero, Designer, ACTgen, ACTmap, Silicon Expert, Silicon Explorer II, Silicon Sculptor, and APSW.

1 Setup

This chapter contains information about setting up Mentor Graphics software to create Actel designs.

Information in this chapter includes software requirements, details regarding how to set up your UNIX account to access Actel and Mentor Graphics software, and details regarding how to launch individual applications using the Mentor Graphics Design Manager icons. Refer to the Mentor Graphics documentation for detailed information about using Mentor Graphics software.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R1-2002 or later and the following third-party software:

- **Mentor Graphics software,** including Design Architect, DVE, QuickSim II, and QuickPath.
- **Synopsys Integrator,** required for integrating Synopsys designs with Mentor Graphics using Actel libraries.

For specific information about which versions this release supports, go to the Guru automated technical support system on the Actel web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

User Setup

Before you create designs with the Actel library, you must set up your account to properly access the Actel and Mentor Graphics software. The following sections describe how to configure your user account for Designer Series in the Mentor Graphics environment for the C-Shell.

Note: For Designer Series environment setup, refer to the *Getting Started User's Guide* and *Designer User's Guide*.

Creating an MGC Location Map File

The MGC Location Map file is an ASCII file that maps soft prefixes to hard path names. It allows flexibility in managing designs in both homogeneous and heterogeneous networks. With location maps, you can move designs to different directories and/or different workstations without changing internal design references.

The Mentor Graphics tools require the MGC Location Map file to determine relative path names. The Mentor Graphics and Actel tools locate this file with the MGC_LOCATION_MAP environment variable. Other variables, including the $MGC_GENLIB variable, are declared in the MGC Location Map file.

The MGC Location Map file is user definable. The name that you give this file is inconsequential, as long as you reference its locations correctly in the MGC_LOCATION_MAP environment variable. For details, see "Configuring User's Accounts for the C-Shell" on page 5.

To create an MGC Location Map file,

follow the design of the listing for the MGC_LOCATION_MAP file provided as follows:

```
MGC_LOCATION_MAP_1
$ALSDIR
<alsdir>
$MGC_GENLIB
<mentor_lib_dir>/gen_lib
$MYDESIGNS
<project_dir>
```

For Design Manager encapsulation, include the following:

```
$ALS_TOOLBOX
<alsdir>/lib/mgc/toolbox
```

For more information regarding location maps, refer to your Mentor Graphics documentation.

Mentor Graphics Library Organization

In addition to the standard Actel libraries, Actel provides a set of migration macros. These are macros supported in earlier versions of the Designer Series software and macros possibly needed to retarget designs to a different Actel family. Actel does not recommend using migration macros in new designs

Standard libraries

In the Mentor Graphics design kit, standard libraries are in $ALSDIR/lib/mgc/<act_fam>. Migration macros are in different locations for different families. For families that did not exist as of Actel Software release R1-1998 and later, migration macros are in $ALSDIR/lib/mgc/<act_fam>_mig.

Legacy library

Migration macros are included in the legacy library for families that existed as of Actel Software release R1-1998. The legacy library is a single, shared library located in $ALSDIR/lib/me. The legacy library was the only Mentor Graphics library in Actel Software releases before R1-1998. You may still use the legacy library for old designs. You may mix blocks containing legacy macros with blocks containing macros from the standard library.

Environment Variable Summary Check List

Before you continue, make sure that you have set the necessary environment variables.

Table 1-1, “Environment Variables,” shows the variables for all UNIX shell types. For details, see “User Setup” on page 1.

Table 1-1. Environment Variables

Variable	Description
☐ ALSDIR	The directory where you have installed the Designer software.
☐ MGC_HOME	The directory where you have installed the Mentor Graphics software.
☐ PATH	The path to access the Designer Series and Mentor Graphics binary files.
☐ AMPLE_PATH	The directory where you have installed the Actel userware. Directory path is as follows: **$ALSDIR/lib/mgc/userware**
☐ MGC_LOCATION_MAP	The MGC location MAP file.
☐ TYPE_REGISTRY	The file that contains the registry types for Design Manager. Directory path is as follows: **$ALSDIR/lib/mgc/als.rgy**
☐ MGC_WD	Optional working directory.

Table 1-2, “MGC Location Map File Variables,” shows the variables for the MGC Location Map File. For details, see “Creating an MGC Location Map File” on page 2.

Table 1-2. MGC Location Map File Variables

Variable	Description
$ALSDIR	The directory where you have installed the Designer Series software.
$MGC_GENLIB	The directory where you have installed the Mentor Graphics generic libraries.
$MYDESIGNS	The directory where your user-design subdirectories reside.
$ALS_TOOLBOX	The directory that contains the Actel toolbox components for Design Manager. Directory path is as follows: **$ALSDIR/lib/mgc/toolbox**

Configuring User’s Accounts for the C-Shell

This section describes how to configure accounts for the C-Shell.

You configure accounts by setting various environment variables. You set these environment variables by editing either the “.cshrc” file, or the “.login” file (not both) to include the following:

```
setenv ALSDIR <alsdir>
setenv MGC_HOME <mentor_install_dir>
set path = ($ALSDIR/bin $MGC_HOME/bin $path)
setenv AMPLE_PATH $ALSDIR/lib/mgc/userware
setenv MGC_LOCATION_MAP <mgc_loc_map_file>
```

To access Design Manager icons, include the following:

```
setenv TYPE_REGISTRY $ALSDIR/lib/mgc/als.rgy
```

Designer Series Mentor Graphics Symbol Libraries

Actel provides symbol libraries specificially for Mentor Graphics. The Designer Series symbol libraries appear in the Design Architect library pull-down menu as Actel Libraries.

The Designer Series library components are in the "$ALSDIR/lib/mgc/<act_fam>/parts" directory.

After selecting Actel Libraries, you can select a family library menu.

When designing with Actel's software, you must use the Mentor Graphics Genlib library components. To do so, you must install the "gen_lib" directory. This library includes bus rippers, portin and portout symbols, etc.

Design Manager Encapsulation Flow

Designer supports Mentor Graphics Design Manager. The Design Manager allows you to invoke the individual applications by selecting and clicking appropriate icons. You need to enter the following commands at the prompt before you invoke the Design Manager:

```
xset +fp $ALSDIR/lib/mgc/fonts
xset rehash
```

Table 1-3, "Mentor Graphics Icons," shows the icons displayed with Design Manager:

Table 1-3. Mentor Graphics Icons

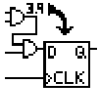
Icon	Description
 act_gen	Invokes ACTgen, which allows designers to create their own macros for use within Design Architect.
 act_edn2mgc	Converts edif to Mentor Graphics netlists for use in Design Architect, QuickSim II, and other Mentor Graphics applications. You can generate a symbol for the netlist using Design Architect's symbol generation.
 act_da	Invokes Design Architect.
 act_presimvpt	Creates a viewpoint for use in Quicksim II. This step is only required for functional simulation of designs that use the legacy library. Refer to "Mentor Graphics Library Organization" on page 3 for further information.
 act_mgc2edn	Creates an edif netlist from a Mentor design for use in Actel's Designer.

Table 1-3. Mentor Graphics Icons (Continued)

Icon	Description
	Creates an adl netlist from a Mentor design for use in Actel's Designer. For Designer 3.0 and above, mgc2edn replaces this step.
	Creates a VHDL file from DA design for use in QuickHDL or ModelSim.
	Invokes Designer, Actel's software to place and route your design for an Actel device.
	Creates QuickSim II- and QuickPath-compatible delay files for back annotation.

2

Actel-Mentor Graphics Design Flow

This chapter describes the design flow for creating Actel designs using Mentor Graphics Design Architect schematic capture tool, QuickSim II simulator, and Actel Designer.

Schematic-Based Design Flow Illustrated

Figure 2-1 shows the schematic-based design flow for an Actel FPGA using Designer software and Mentor Graphics software.[1]

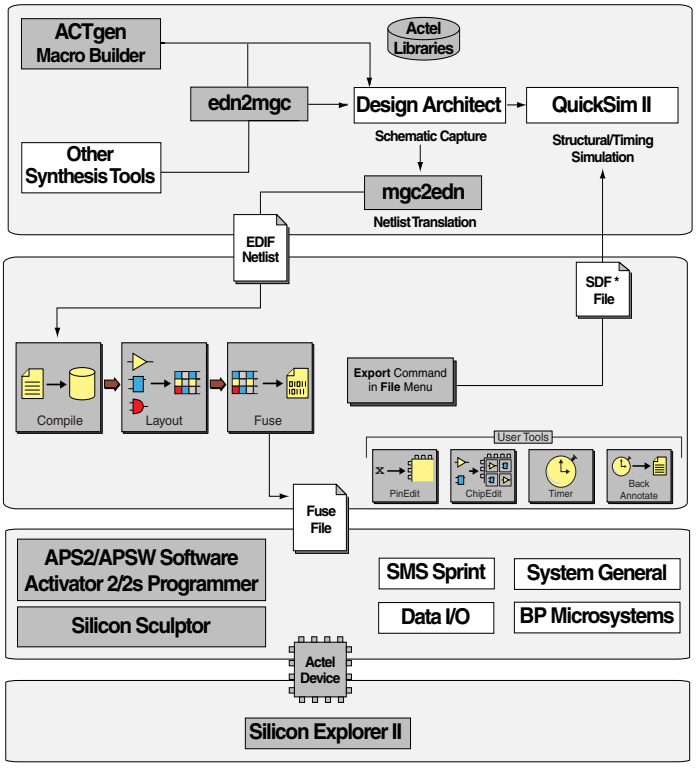


Figure 2-1. Schematic-Based Design Flow

1. The grey boxes in Figure 2-1 denote Actel-specific utilities/tools.

Schematic-Based Design Flow Overview

The following describes the design flow for creating a design using the Design Architect Schematic capture program, QuickSim II simulator, and Actel Designer Series software. For instructions on how to use the Designer Series software and its tools, refer to the *Designer User's Guide*.

Design Creation/ Verification

The following describes Design Creation/Verification.

Schematic Capture

Enter your design in Design Architect. Use one of the Actel family symbol libraries. Save the design. Refer to Mentor Graphics documentation for more information.

EDIF Netlist

After you create the schematic, use mgc2edn to create an EDIF ".edn" netlist. Refer to "Creating an EDIF Netlist" on page 22 for more information.

Functional Simulation

Use QuickSim II to perform a functional simulation of your design. Refer to Mentor Graphics documentation for more information.

Note: The functional simulation sets all delays to one nanosecond.

Design Implementation

During design implementation, you use Designer to place-and-route a design. Additionally, you may perform static-timing analysis in Designer with the Timer tool. After place-and-route, you perform postlayout (timing) simulation with QuickSim II.

Place-and-Route

Use Designer to place-and-route your design. Refer to the *Designer User's Guide* for information about using Designer.

Timing Analysis

Use the Timer tool in Designer to perform static-timing analysis on your design. Refer to the *Timer User's Guide* for information about using Timer.

You can also perform static-timing analysis using Mentor Graphics QuickPath. Refer "Static-Timing Analysis Using QuickPath" on page 33 for more information.

Timing Simulation

You perform a timing simulation on your design using QuickSim II after placing-and-routing it. Timing simulation verifies that the design meets your timing requirements. Timing simulation requires information extracted and back annotated from Designer. Refer to "Timing Simulation with SDF Back Annotation" on page 25 for detailed information.

Note: QuickSim and QuickPath are not supported for the Express family.

Use Verilog or VHDL simulators, along with the Verilog or Vital libraries, for your design targeted for the Express family.

Programming

You program a device with programming software and hardware from Actel or a supported third-party programming system. Refer to the *Designer User's Guide* and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information on programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information about using the Silicon Explorer.

3

Actel-Design Architect Design Considerations

This chapter describes various conventions to observe when creating a design for Actel devices using Mentor Graphics Design Architect. Included in this chapter are details about schematic naming conventions, designing using multiple page designs, adding input and output macros to your desgin, adding ACTgen macros, and adding Synopsys blocks. Also included is information about creating an EDIF netlist and importing an EDIF netlist into Mentor Graphics.

Schematic Naming Conventions

You can add a new set of Actel properties to schematics in Mentor Graphics' Design Architect. Once you attach a property to a net or an instance, the property name and value will propagate to the proper location in the Actel design files.

When creating a schematic for Actel devices, you must observe the conventions described in the following sections.

Specifying Properties in Design Architect

You can assign properties on the desired object directly in the schematic. After saving the design, the "netlist" command (mgc2edn) reads the schematic and attaches the property name and value to the corresponding net in the .edn file.

Follow the procedure below to add a net property in the schematic:

1. **Open the schematic in Design Architect.**
2. **Select one end of the NET.**
3. **Choose the "Add" command from the "Properties" menu.** A new menu will appear.
4. **For the "property name" type the property name.** For example:

   ```
   alspin
   ```

5. **For the "property value" enter the property value.** Refer to Table 3-1 for a description of the available Properties.
6. **Select "OK" and attach the property to the Net.**

Naming Conventions

Use only alphanumeric and underscore "_" characters for schematic net and instance names.

Note: Do *not* use asterisks, forward and backward slashes, or spaces.

Top-Level Symbol

You may create a top-level symbol for the entire design. The pin names on the symbol must match the underlying dangling net names on the top-level schematic or the symbol "portin/portout" names on the I/O pads. Remember to update the symbol if the pins on the schematic change. If a top-level symbol is not created, you must use portin/portout from Genlib on all of the I/O pins.

Note: The top-level symbol must contain only pins for I/O buffers. Do not add power, ground, pra, or prb pins, etc. to the symbol. Doing so will cause errors during netlisting.

Preserve

One of the Combiner's functions is to combine (optimize) combinatorial functions into sequential macros for Actel device families. Combining logic does not affect the function of the circuit. To prevent such combining, you may add an ALSPRESERVE property to the net connecting the macros that would otherwise be combined. The ALSPRESERVE property information is copied into the <design_name>.edn (see Table 3-1).

Table 3-1. Properties

Property Name	Property Value	Attached to
ALSPIN	package pin number	NET (net connecting a port with an I/O buffer)
ALSPRESERVE	(none)	NET (any net)

Multiple-Page Design

For a multiple-page design, treat each sheet as a part of a schematic and do not consider it as a level of hierarchy. Use “offpag.in” and “offpag.out” connectors to connect sheets.

Adding Input and Output Macros

This section describes adding input and output macros.

Adding I/O Pins to the Schematic

The procedure for adding I/O buffers is to place the buffer on the schematic sheet and add a net to the pad side of the buffer as shown in Figure 3-1. Then, you can attach either an MGC Genlib component, portin or portout, to the net and label it or the existing net. Actel recommends placing all Input and Output buffers on the top-level sheet of the design. If the Input and Output buffers are buried within the design, you must pull a net for every I/O signal to the top-level sheet and connect it to the corresponding port. If you do not use portin and portout, you must create a top-level symbol that contains a pin for every I/O buffer.

The labels attached to the net or portin or portout will appear as pin names in Pin Edit.

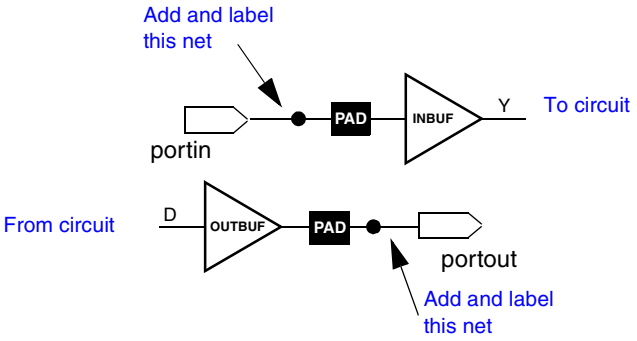


Figure 3-1. I/O Pins in a Mentor Graphics Design

Assigning I/O Pins to the Schematic

One way of assigning I/O pins is to use Pin Edit within Designer. Another way is to assign a property (a pin property called ALSPIN with the corresponding package pin number) to the net connecting a port to an I/O buffer, as shown in Figure 3-2.

The labels attached to the net or portin or portout will appear as pin names in Pin Edit.

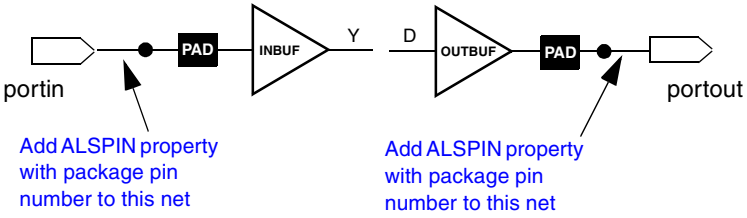


Figure 3-2. Adding I/O Pins to a Mentor Graphics Design

Note: PinEdit does not change the Mentor Graphics netlist or schematic information. Pin locations modified with PinEdit are not back annotated to the schematic.

Adding ACTgen Macros

With the ACTgen Macro Builder, you can create macros using a simple description. The ACTgen Macro Builder can produce counters, adders, decoders, RAM, and FIFO in a very short time. In addition, you can easily integrate ACTgen-based blocks with schematics and symbols into a Mentor Graphic's Design Architect design.

ACTgen Macro Generation

To integrate a macro generated using ACTgen with schematic capture using Design Architect, instantiate the generated symbol into your design.

Generating an ACTgen Macro

Refer to the *Designer User's Guide* for information regarding using the ACTgen software. Be sure to specify MGC as the CAE type.

Instantiating the Macro

Perform the following steps to instantiate a macro generated by ACTgen.

1. **In Design Architect, choose the "Symbol By Path" command from the "Instance" pop-up menu.** Use the navigator to instantiate the symbol. The symbol is instantiated from its directory and should appear on the schematic sheet. Place it on the sheet by clicking the left mouse button.
2. **Complete the <design_name> by adding the rest of the schematic components, including I/O buffers, CLKBUF (if a clock signal is present) from the Actel Library, and Portins and Portouts from Mentor Graphics Genlib library.** Check and save the <design_name> design.

   Note: ACTgen expects the macro to be generated within your design directory. For example, if your design is called design_name, ACTgen expects to create the macro under the design_name directory. After creation, ACTgen will create the file design_name/<macro_name>.gen.
3. **Exit Design Architect.**

Adding Synopsys Blocks

One technique in the EDA environment is integrating Synopsys with Mentor Graphics. The Synopsys Integrator for Falcon Framework is a tool that allows you to build a design in HDL, optimize the design with Synopsys, and convert the design from a Synopsys database to a Mentor Graphics database for simulation.

Synopsys Integrator interacts with the Mentor Graphics database. When the tool is loaded and all variables are set, you can perform the database translation with the Mentor Graphics Design Manager.

In this section, we discuss how to:

- Set the Synopsys Integrator environment variables.
- Start the Design Manager to display the Synopsys tools.
- Generate a Synopsys-/Mentor Graphics-compatible symbol library.
- Transfer a design from the Synopsys database to the Mentor Graphics database.

Environment Setup

Before starting the integration, you must verify that the search path is set to access the Falcon Framework software. Furthermore, you must define the following three environmental variables to run the Synopsys Integrator software from the Mentor Graphics environment:

```
$SYNOPSYS_IFF_ROOT
$TYPE_REGISTRY
```

You must set the "$SYNOPSYS_IFF_ROOT" variable in the location map file and in your ".kshrc," ".profile," or ".cshrc" start-up files. You must set the "$SYNOPSYS_IFF_ROOT" variable to the directory where the Synopsys Integrator is installed. For example, set the "$SYNOPSYS_IFF_ROOT" variable to:

```
$SYNOPSYS/platform/syn/interfaces/mentorA
```

In our example, "$SYNOPSYS" is the directory where the Synopsys software is installed, and "platform" can be either the "hp700" or "sparc" directory, depending on your workstation.

You must set the "$TYPE_REGISTRY" in the location map file and your ".kshrc," ".profile," or ".cshrc" start-up files. This variable must be equal to the following directory:

```
$SYNOPSYS_IFF_ROOT/registry/synopsys.rgy
```

Design Manager Setup

Invoke Design Manager by typing the following:

```
dmgr
```

To create the Synopsys icons, follow the procedures below:

1. **In the Tools window, click the right mouse button to display the Tool Operation pop-up menu.**
2. **From the Tool Operation pop-up menu, select View Toolboxes to display the Toolboxes window.**
3. **From the Toolboxes pop-up menu, select Add Toolbox to display the ADD TO prompt bar.**
4. **In the ADD TO prompt bar, type "$SYNOPSYS_IFF_ROOT/toolbox," and press Return or click OK.**
5. **From the Toolboxes pop-up menu, select Save.** This adds the Synopsys toolbox path to the Mentor Graphics start-up file located in the "user_directory/mgc/startup/dmgr_toolbox_path.startup" file.
6. **From the Toolboxes pop-up menu, select View Tools.** The Tools window displays the Synopsys tools at the bottom of the window.
7. **From the "Setup" menu, choose the "Icon Layout" command.** This rearranges the icon location in the Tools window.
8. **Close and exit the Mentor Graphic Design Manager.**

DB2EDDM Database Translation

A description of how to transfer a design from the Synopsys database to the Mentor Graphics database follows below.

To create a Mentor-compatible schematic, follow the procedures below:

1. **Set the symbol_library variable in the ".synopsys_dc.setup" file to the "*fam*_mntr.sdb" library.** If you set the symbol library to the Actel-Synopsys symbol library, the symbols in Mentor will be offset.
2. **Read in a VHDL design or "design.db" file in Synopsys.**
3. **Execute the "mgc_name.scr" script file found in the "<synopsys_syn_lib_loc>/scripts/<act_fam>" library directory.**
4. **Save design as "design.db."** If you do not wish to override your old "design.db" file, save the design with a different name.
5. **Invoke Design Manager by typing the following**

   ```
   dmgr
   ```

6. **From the Tools window, double-click on the "db2eddm" icon.** This opens the Synopsys DB to EDDM window (Figure 3-3**).**

In the Synopsys DB to EDDM window, follow the procedures below:

1. **In the DB File field, type the "<design>.db" design name.**
2. **In the Add Search Path field, type the hard path to the location of the "<design>.db" file.**
3. **In the Map File field, type the hard path and the map file name "<act_fam>.map."** You set the output directory by default to the location of the "design.db" file.

4. **Click OK.** This launches the “db2eddm” program**.**

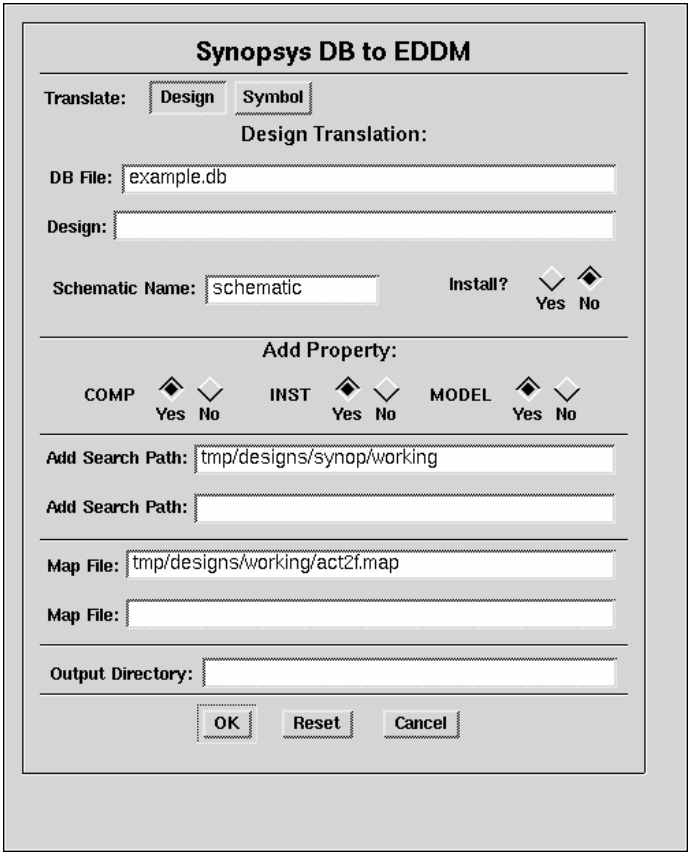


Figure 3-3. Synopsys DB to EDDM Window

Note: The following screen messages could appear:

```
Warning: Can't locate file `actsym.sdb' (DB-3)
```

```
Error: can't find symbol for instance xxx of design
```

If the preceding messages do appear, set the “symbol_library” variable in the “.synopsys_dc.setup” file to the “<act_fam>_mntr.sdb” file location.

5. **To review your design results, invoke Design Architect and read in the schematic sheet.**

The above conversion process is not fully qualified for Synopsys versions 97.01 and after. The recommended way to create an EDDM database is to begin with an EDIF file and then invoke the “act_edn2mgc” icon from the Design Manager or run the “edn2mgc” from the project directory as follows:

```
edn2mgc fam:<act_fam> <design_name>
```

Creating an EDIF Netlist

After entering the schematics and functionally simulating the design, create the EDIF netlist file, <design_name>.edn, which you will import into Designer. The Actel command that generates EDIF netlist is “mgc2edn.”

Invoke the “act_mgc2edn” icon from Design Manager or from the project directory, type the following:

```
mgc2edn fam:<act_fam> <design_name>
```

Creating an HDL Netlist

The command that generates a VHDL netlist is “mgc2vhdl.”

Invoke the “act_mgc2vhdl” icon from the Design Manager or from the project directory, type the following:

```
mgc2vhdl fam:<act_fam> <design_name>
```

The command that generates a verilog netlist is “mgc2vlog.”

To invoke this command from the project directory, type the following:

```
mgc2vlog fam:<act_fam> <design
```

Importing an EDIF Netlist

You can import an EDIF netlist generated by other CAE tools into the Mentor Graphics design database EDDM for simulation with QuickSim II and/or timing analysis with QuickPath.

To import a netlist into Mentor Graphics, invoke the “edn2mgc” command from the Design Manager window or from the project directory, type the following:

```
edn2mgc fam:<act_fam> <design_name>
```

Note: The “edn2mgc” utility only reads EDIF netlists with supported flavors. To work around the unsupported EDIF, run “edn2adl” and then run “adl2edn” to obtain an EDIF netlist with Actel Flavor. Then, run “end2mgc.”

If you are running “edn2mgc” on the EDIF netlist created with Designer 3.1.1 or earlier, you may observe the following error message:

```
Error: Could not find external part.
```

If you get this error message, it is because these missing macros are not supported in the standard library. Call Actel Customer Applications Center to request the migration library. Refer to “Product Support” on page 31 for information about contacting Actel Customer Applications Center.

4

Simulation Using QuickSim II

This section describes steps to perform functional simulation (behavioral and structural), timing simulation, and board-level simulation for Actel devices using the Mentor Graphics QuickSim II simulator.

Note: QuickSim II is not supported for the Express family.

Use Verilog or Vital libraries for your design targeted for the Express family.

Functional Simulation

To simulate your design with unit delays, run Quicksim II by typing the following:

```
quicksim <design_name>
```

Note: If your design uses the legacy library (as described in "Mentor Graphics Library Organization" on page 3) you need to run the following command pior to running your first functional simulation:

```
presimvpt fam:<act_fam> <design_name>
```

If your design does not use the legacy library, "presimvpt" need not be run.

Timing Simulation with SDF Back Annotation

To simulate with SDF back annotation, extract the SDF file from Designer and perform the following steps:

1. **Type the following:**

   ```
   quicksim <design_name> -tim max
   ```

2. **In the QuickSim II window, choose Load SDF from the File menu, then specify the SDF file name for back annotation.**

Note: Back annotation with SDF is supported with only Mentor Graphics software versions B.1 or later.

Board-Level Simulation

System designs are typically divided into functional modules that several Actel devices implement. To check the functionality of the system, it is very important to simulate all of the Actel devices together. The Actel Designer Series system includes board-level, multichip simulation capability using Mentor Graphics software for Actel devices.

The software requirements are identical for chip-level and board-level simulations. The requirements are Mentor Graphics' Design Architect (DA), Design Viewpoint Editor (DVE), Quicksim II, and Actel's Designer Series Development System.

Board-Level Design Example

This section assumes that you know how to use Design Architect to create symbols and sheets for your chip-level designs. Consider the board level design, "board," which contains the chip-level components *chip1, chip2* and *chip3*. Each component is composed of a symbol and a schematic.

In this example, the *board* schematic includes *chip1, chip2* and *chip3* symbols, which are ACT 1, ACT 2, and ACT 3 family designs, respectively. Figure 4-1 shows the "board" design.

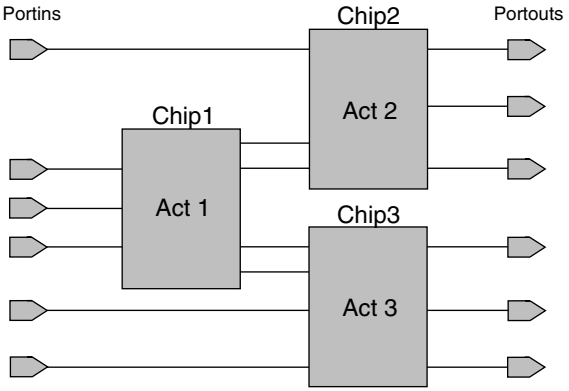


Figure 4-1. Board Schematic Sheet

To create a netlist for *chip1*, perform the following steps:

1. **Run "mgc2edn" on the design to generate the Actel netlist by typing the following command:**

   ```
   mgc2edn fam:<act_fam> chip1
   ```

2. **Create the back-annotation (*.sdf) file for *chip1*.** Use Designer to layout and extract postlayout delays for the device.

   This step creates the back-annotation file, "chip1.bao."

   Note: Before you continue, repeat steps 1 and 2 for all chips in your design.

3. **To create the schematic sheet "board" in Design Architect, perform the following steps:**

   - From the "Instance" pop-up menu, select the "Choose Symbol" command.
   - Use the Navigator to select and place *chip1* on the schematic sheet. Repeat this procedure for all chips in your design.

- Connect the symbols and add Portins and Portouts to the schematic.
- Execute the “Check Sheet” command and save the changes.
- Open a new symbol sheet and create the board symbol.
- Execute the “Check Sheet” command and save the changes.

4. **Enter the following command to invoke QuickSim II with back-annotated delays.**

```
quicksim <board> -tim max
```

To load the SDF files of all the chips in your design:

- Choose the load SDF from the file menu, then specify the SDF file for chip1.
- Repeat the process for all the chips in your design.

Note: Specify the correct instance name while loading an SDF file for each instance.

5

Static-Timing Analysis Using QuickPath

This chapter describes how to perform static-timing analysis using QuickPath. Refer to the Mentor Graphics QuickPath documentation for more information about QuickPath.

Note: QuickPath is not supported for the Express family.

Timing Analysis with SDF

After extracting the .sdf file from Designer, execute the timing analysis by performing the following steps:

1. **Invoke QuickPath by typing:**

   ```
   quickpath <design_name>
   ```

2. **Choose the "Load.SDF" command from the File menu and select the .sdf file for back annotation.**

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for nontechnical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1256 305600.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Customer Applications Center

Actel staffs its Customer Applications Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Applications Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your question(s).

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (**http://www.actel.com/guru/**). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and nontechnical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is **http://www.actel.com**. You are welcome to share the resources provided on the Internet.

Be sure to visit the Technical Documentation area on our web site, which contains information regarding products, technical services, current manuals, and release notes.

You can visit the Product Support area of the Actel website from your Designer software. Click the Product Support button in your Designer Main Window to access the latest datasheets, application notes, and more.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. Here you can obtain library updates, software patches, design files, and data sheets.

Contacting the Customer Applications Center

Highly skilled engineers staff the Customer Applications Center from 7:30 A.M. to 5:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Message Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 A.M. to 5:00 A.M., Pacific Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

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