# *Actel® Tools*

## *Netlist Viewer User's Guide*
## *R1-2003*

*Windows® & UNIX® Environments*

**Actel® Corporation, Sunnyvale, CA 94086**


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Trademarks

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# Introduction

The Netlist Viewer displays your netlist in a hierarchical manner, providing you with a logical view of your design.

The Netlist Viewer can be used alone to explore each level of the hierarchy and to trace signals. Used with PinEdit, ChipEdit, or Timer, the Netlist Viewer assists you in meeting area and timing goals by helping you with critical path identification.

## Document Organization

This guide provides detailed cross-platform information about Netlist Viewer. Use it as a reference in your everyday work.

Step-by-step instructions for using Netlist Viewer on Windows and UNIX workstations are in this guide. Any platform differences in procedures and commands are noted in the text.

The Netlist Viewer User's Guide contains the following chapters:

**Chapter 1 - Getting Started with Netlist Viewer** contains details about Netlist Viewer's interface, toolbars, and menu commands.

**Chapter 2 - Using Netlist Viewer** contains instructions on how to use Netlist Viewer alone, or with other User Tools to locate paths.

**Chapter 3 - Examples** illustrates common uses for the Netlist Viewer.

**Appendix A - Product Support** provides information about contacting Actel for customer and technical support.

## Document Assumptions

This document assumes you have a working knowledge of your operating system and its conventions, including standard menus and commands, how to use a mouse, and how to open, save, and close files. For help with any of these techniques, see the documentation that came with your computer.

This document also assumes you are familiar with the FPGA architectures and have a working knowledge of the Designer software.

# Actel Manuals

Designer and Libero include printed and online manuals. The online manuals are in PDF format and available from Libero and Designer's Start Menus and on the CD-ROM. From the Start menu choose:

- Programs > Libero 2.2 > Libero 2.2 Documentation.
- Programs > Designer Series > R1-2002 Documentation

Also, the online manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the online manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

The Designer Series includes the following manuals, which provide additional information on designing Actel FPGAs:

*Libero User's Guide.* This manual contains information about using Libero, Actel's Integrated Design Environment. Details about using ViewDraw for Actel, WaveFormer Lite, Synplicity, and ModelSim are provided.

*Getting Started User's Guide.* This manual contains information for using the Designer Series Development System software to create designs for, and program, Actel devices.

*Designer User's Guide.* This manual provides an introduction to the Designer series software as well as an explanation of its tools and features.

*PinEdit User's Guide.* This guide provides a detailed description of the PinEdit tool in Designer. It includes cross-platform explanations of all the PinEdit features.

*ChipEdit User's Guide.* This guide provides a detailed description of the ChipEdit tool in Designer. It includes a detailed explanation of the ChipEdit functionality.

*Timer User's Guide.* This guide provides a detailed description of the Timer tool in Designer. It includes a detailed explanation of the Timer functionality.

*SmartPower User's Guide.* This guide provides a detailed description of using the SmartPower tool to perform power analysis.

*Netlist Viewer User's Guide.* This guide provides a detailed description of the Netlist Viewer. Information on using the Netlist Viewer with Timer and ChipEdit to debug your netlist is provided.

*A Guide to ACTgen Macros.* This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

*Actel HDL Coding Style Guide.* This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

*Silicon Expert User's Guide.* This guide contains information to assist designers in the use of Actel's Silicon Expert tool.

*Cadence® Interface Guide.* This guide contains information to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

*Mentor Graphics® Interface Guide.* This guide contains information to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

*Synopsys® Synthesis Methodology Guide.* This guide contains preferred HDL coding styles and information to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

*Synplicity Synthesis Methodology Guide.* This guide contains information about using the Synplicity Synthesis tools with Actel Designer Series software to create designs for Actel devices.

*Innoveda® eProduct Designer Interface Guide (Windows).* This guide contains information to assist designers in the design of Actel devices using eProduct Designer CAE software and the Designer Series software.

*VHDL Vital Simulation Guide.* This guide contains information to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

*Verilog Simulation Guide.* This guide contains information to assist designers in simulating Actel designs using a Verilog simulator.

*Activator and APS Programming System Installation and User's Guide.* This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

*Silicon Sculptor User's Guide.* This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

*Flash Pro User's Guide.* This guide contains information about how to program Actel ProASIC and ProASIC PLUS devices using the Flash Pro software and device programmer.

*Silicon Explorer II.* This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

*Macro Library Guide.* This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

*WaveFormer Lite Guide.* This guide contains information on using WaveFormer Lite to generate VHDL and Verilog stimulus based test benches for the Actel design software.

*ViewDraw User's Guide.* This guide contains information about using ViewDraw.

*ModelSim Bookshelf.* This bookshelf contains the ModelSim User's Guide, Command Reference, and Tutorial.

## Online Help

The Designer Series software comes with online help. Online help specific to each software tool is available in Libero, Designer, ChipEdit, PinEdit, Libero, ACTgen, Silicon Expert, Silicon Explorer II, Silicon Sculptor, and APSW.

# 1

# Getting Started with Netlist Viewer

This chapter contains details about Netlist Viewer's interface and commands. For information on using Netlist Viewer with PinEdit, ChipEdit, or Timer, see

## Starting Netlist Viewer

Netlist Viewer is available from Designer's main window. It can only be started after your design has been compiled.

To start Netlist Viewer from Designer, click *Netlist Viewer*, as shown in Figure 1-1. If you have not compiled your design, Designer prompts you to go through the compilation process.


*Figure 1-1. Netlist Viewer Button*

The Netlist Viewer reads in your netlist design and generates a clearly laid out schematic view, as shown in Figure 1-2.

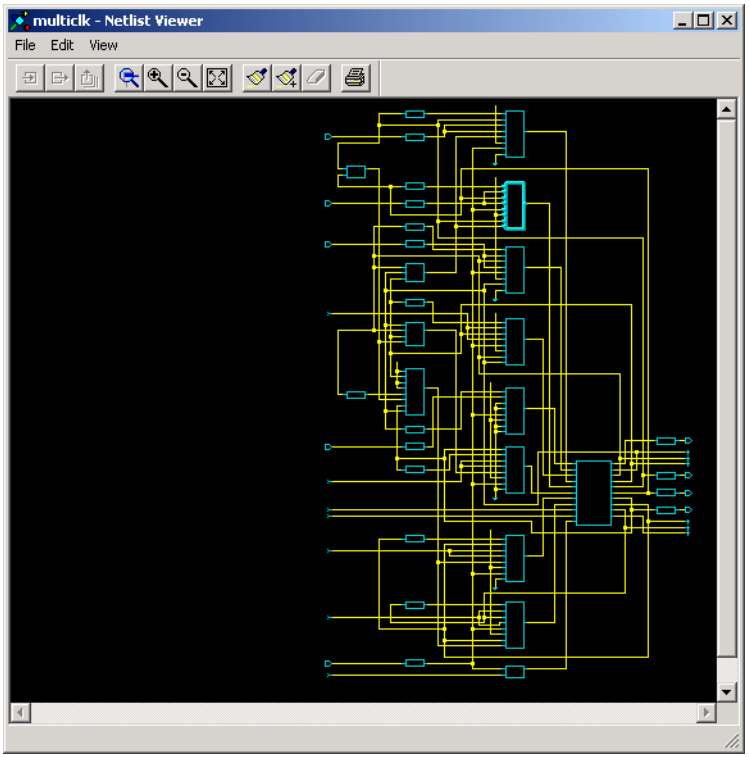



*Figure 1-2. Netlist Viewer*

# Netlist Viewer

The Netlist Viewer, as shown in Figure 1-3, consists of three windows, the Schematic View, Hierarchical View, and Search View Windows. The Netlist

Viewer also contains a menu bar, toolbar, and status bar. Each of these items is described below.

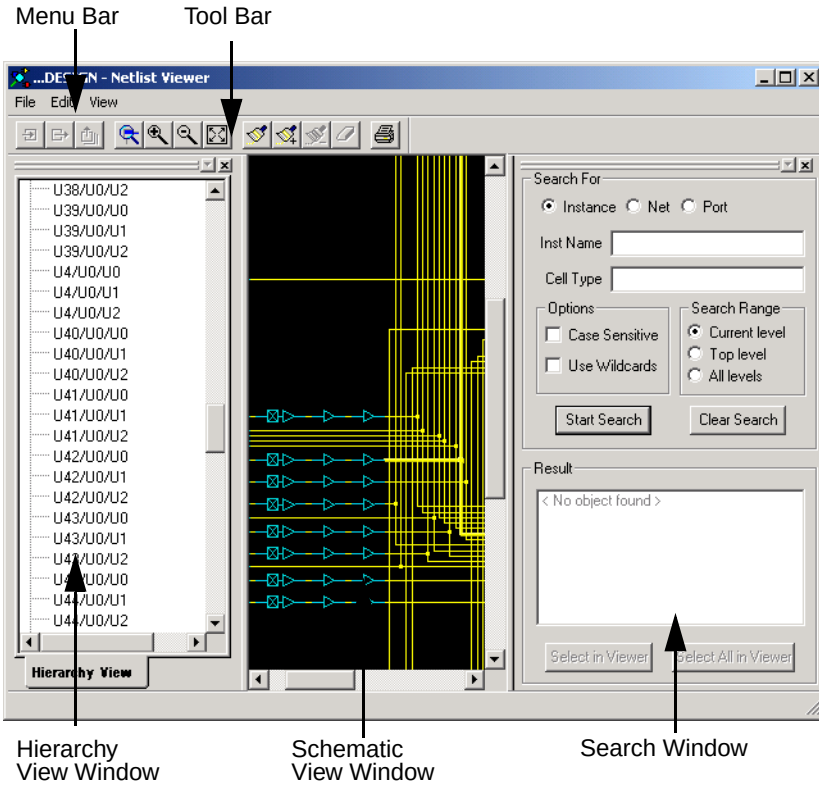



*Figure 1-3. The Netlist Viewer With All Windows Open*

## Schematic View

The Schematic View Window displays a graphical representation of the netlist.

## Design Hierarchy View

The Design Hierarchy View Window provides easy navigation through the design hierarchy and gives a compact hierarchy overview.

### To view the Design Hierarchy View Window:

1. **From the View menu, click *Hierarchy*.** The hierarchy window opens. This window is sizable and dockable.

Any item selected in one window is selected in all, as shown in Figure 1-4.

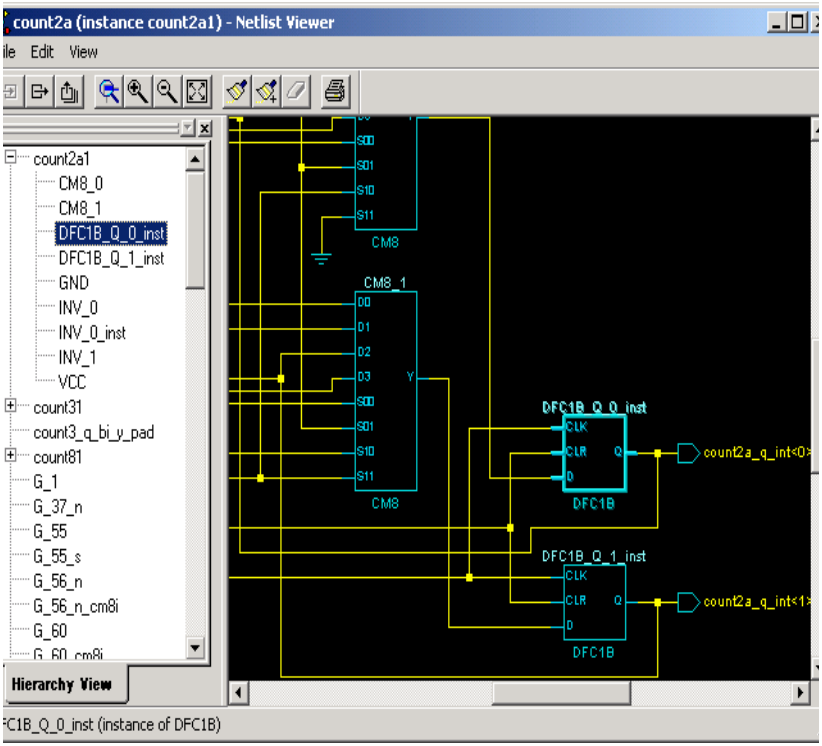



*Figure 1-4. Hierarchy View Window*

## Search View

Use the Search window to search for instances, nets, and ports. For information on using the search view, "Search View" on page 14.

*To open the Search View Window:*

1. **From the View menu, click *Search Tool.*** The Search View Window opens to the right of the Schematic View window, as shown in Figure 1-5.

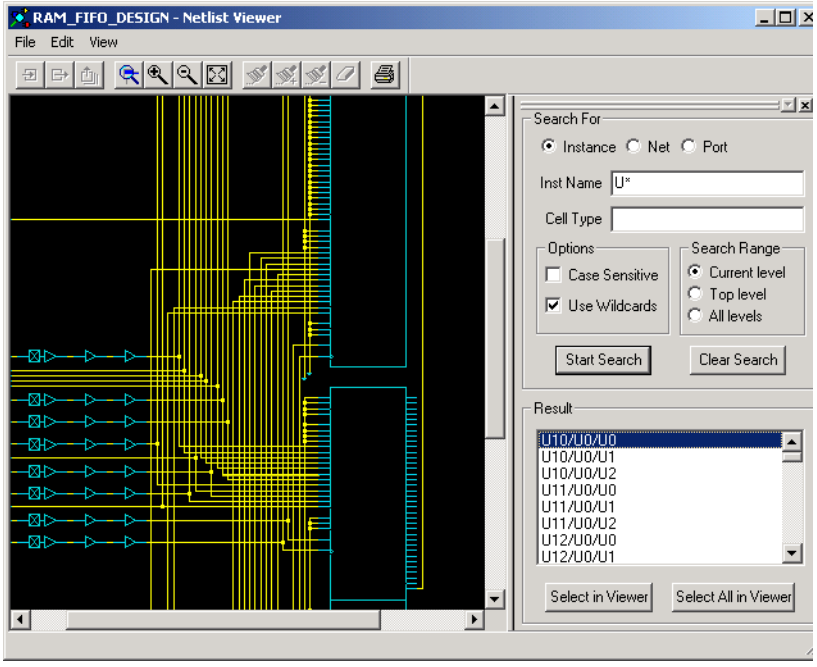



*Figure 1-5. Search View Window*

The Search View Window is sizable and dockable.

# Navigation

You can navigate in the logical view of the design in two directions:

## Vertical

You can navigate vertically if you have a hierarchical design.

Use the Push and Pop commands, from the Edit menu and the toolbar, to move through the hierarchical design. The Push command allows you to go

one level deeper in the design hierarchy. Pop is the reverse action, your view rises up one level.

Right-click anywhere in the Netlist Viewer to open a right-click menu, which provides shortcuts to Push and Pop functions.

The menu and toolbar also include a Top command that brings you back to the top level of the design hierarchy.

All three commands can be accessed through keyboard shortcuts:

- CTRL-P for Push
- CTRL-O for Pop
- CTRL-T for Top

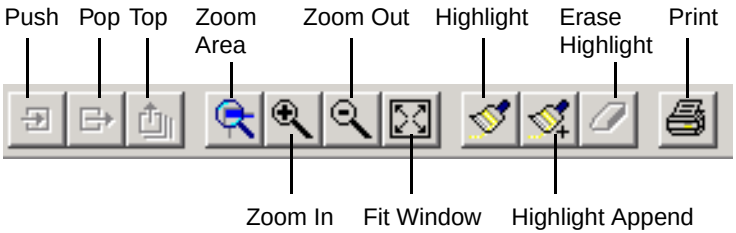
### Horizontal

Large designs might not fit in the window. When this occurs, Netlist Viewer applies page splitting.

Navigate through pages at a given level by following a net. Nets that continue on another page are terminated by special symbols. To follow the net, double-click on the symbol. For more information, refer to "Navigating Through Your Netlist" on page 20.

## Toolbar

Netlist Viewer's toolbar contains commonly used commands.



# Menu Commands

## File Menu

**Print**: Prints what is currently displayed in the Netlist Viewer.

**Print Preview**: Prints what is currently displayed in the Netlist Viewer to a preview window.

**Print Setup**: Sets up your printing options.

**Close**: Closes the Netlist Viewer.

## Edit Menu

**Push**: Displays the next lower level in the design hierarchy.

**Pop**: Displays the next higher level in the design hierarchy.

**Top**: Displays the top level of the design.

**Highlight**: Marks the currently selected object by turning it red.

**Highlight Append**: Highlights the currently selected object, by turning it red, and adds it to a group, which includes that last highlighted object.

**Unhighlight**: Unmarks the selected object only, returning it to yellow or blue.

**Clear Highlight**: Clears all marked objects, returning them to yellow or blue.

## View Menu

**Zoom Window**: Allows you to drag out an area to enlarge.

**Zoom Fit**: Fits design in Netlist Viewer.

**Zoom In**: Magnifies the view by a factor 2 (x2).

**Zoom Out**: Reduces the view by a factor 2 (x.5).

**Redraw**: Redraws the screen.

**Go to First Page**: Takes you to the first page in the design.

**Go to Previous Page**: Displays the previous page in the Schematic View window.

**Go to Next Page**: Displays the next page in the Schematic View window.

**Go to Last Page**: Displays the last page in the Schematic View window.

**Pre-optimized Netlist (Axcelerator Family)**: Displays the pre-optimized netlist in the Schematic View window.

**Optimized Netlist (Axcelerator Family):** Displays the optimized flattened netlist in the Schematic View window. This is the default view.

**Toolbar**: Hides or displays the toolbar.

**Search Tool**: Hides or displays the Search window.

**Hierarchy**: Hides or displays the Hierarchy window.

# 2

# Using Netlist Viewer

The Netlist Viewer can be used alone to explore each level of the hierarchy and to trace signals. Used with PinEdit, ChipEdit, or Timer, the Netlist Viewer assists you in meeting area and timing goals by helping you with critical path identification.

## Viewing Your Netlist

The Schematic View Window displays your netlist in a graphical manner, assisting you in debugging your netlist.

### To view your netlist using Netlist Viewer:

1. **Start Netlist Viewer.** Click *Netlist Viewer* in the Design Flow window. The Netlist Viewer starts and displays your netlist as shown in Figure 2-1.

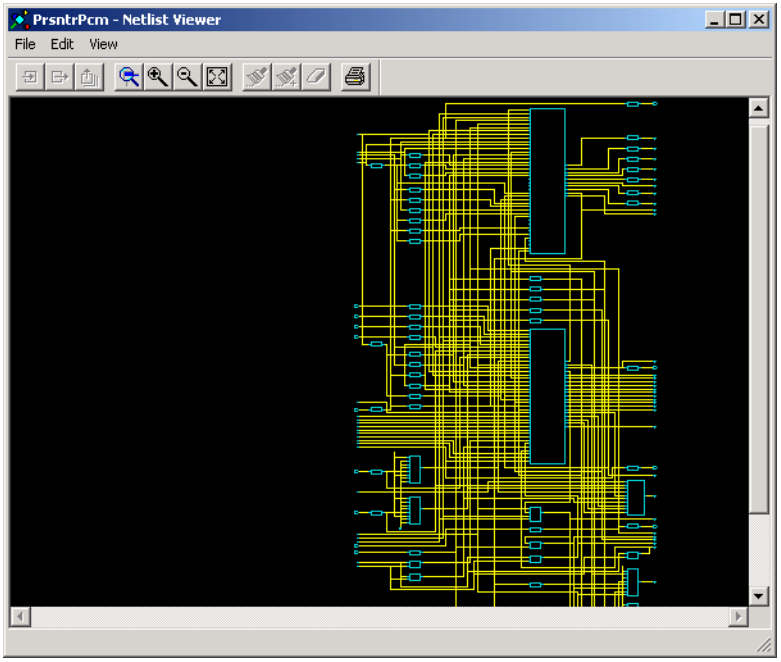



*Figure 2-1. Netlist Viewer Opens*

### Axcelerator Designs

For Axcelerator designs only , choose to view the optimized flattened netlist or the pre-optimized hierarchical netlist.

Both have advantages and weaknesses:

- The optimized flattened netlist is a non-hierarchical view. Use the optimized flattened netlist when cross-probing with other User Tools, such as PinEdit or Timer.
- The pre-optimized netlist is the original netlist, as passed to the Designer software. The hierarchical structure is useful for navigating. When using the pre-optimized netlist for cross-probing, some items might not appear.

To switch between the different views, from the View menu, click *Pre-Optimized Netlist* or *Optimized Netlist*.

## Navigating Through Your Netlist

You can navigate in the logical view of the design vertically and horizontally. This section describes both.

### Vertical Navigation

Vertical navigation is possible for all families and for the Axcelerator family, if you use the pre-optimized netlist. Navigate vertically through your hierarchical design by using the push, pop, and top commands. These commands are available from the Edit menu, the right-click menu, and the toolbar. They can also be accessed through keyboard shortcuts: CTRL-P for Push, CTRL-O for Pop and CTRL-T for Top.

#### To go one level deeper in a design:

1. **Select an instance.**

2. **From the Edit menu, click *Push*. Or, from the right-click menu select Push instance <name>, as shown in Figure 2-2.**

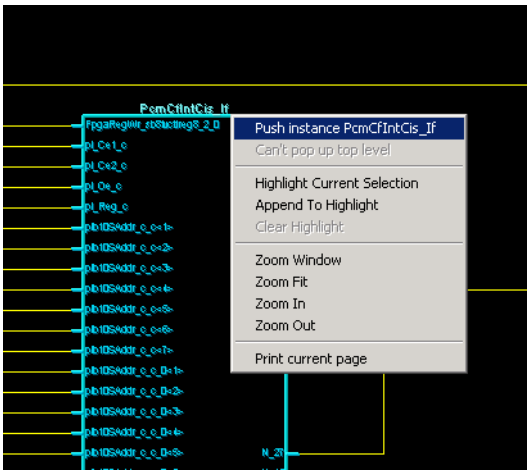



*Figure 2-2. Pushing One Level Deeper into the Design*

### *To rise one level higher in a design:*

1. **From the Edit menu, click *Pop*.**

### *To rise to the top level:*

1. **From the Edit menu, click *Top*.**

## Horizontal Navigation

When large designs do not fit in the Schematic View window, Netlist Viewer applies page splitting.

### *To navigate to the next page in a design do one of the following:*

- From the View Menu, click Go to Next Page
- Click the Next Page button in the toolbar

### To navigate to the previous page:

- From the View Menu, click *Go to Previous Page*
- Click the *Previous Page* button in the toolbar

### To navigate to the first page:

- From the View menu, click *Go to First Page*
- Click the *First Page* toolbar button

### To navigate to the last page:

- From the View menu, click *Go to Last Page*
- Click the *Last Page* toolbar button

## Following Nets

Following a net might take you to the next page in a schematic, or several pages away.

### To follow a net:

- In the Schematic View window, click a net that continues before or after the page being viewed. Nets that continue are terminated by the symbol shown in Figure 2-3. Nets that continue on a previous page are terminated by the symbol shown in Figure 2-4. Click the symbol to follow the net.

*Figure 2-3. Symbol for Continuing Net*

*Figure 2-4. Symbol for Previous Net*

In the example below, Figure 2-5, clicking the symbol next to sclk3m57_0 takes you to the page where the net continues.


*Figure 2-5. Symbol for a Continuing Net*

In the example below, Figure 2-6, clicking the symbol next to sclk3m57_0 takes you to the page where the net came from.

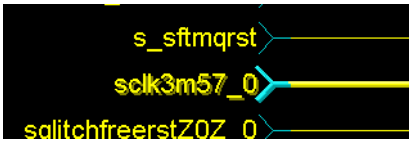



*Figure 2-6. Symbol for Previous Net*

# Using the Design Hierarchy View

The Design Hierarchy View Window provides easy navigation through the design hierarchy and gives a compact hierarchy overview. When an instance is selected in the Design Hierarchy View window it is highlighted in the Schematic View window.

## To view the design Hierarchy View window:

1. **From the View menu, click *Hierarchy*.** The hierarchy window opens.
2. **Select an instance name in the hierarchy.** The instance is located and highlighted in the Schematic Viewer, as shown in Figure 2-7. All parents as well are selected. Since any item selected in one window is selected in all,

selecting an instance in the Schematic Viewer locates and selects the instance in the Hierarchy View.

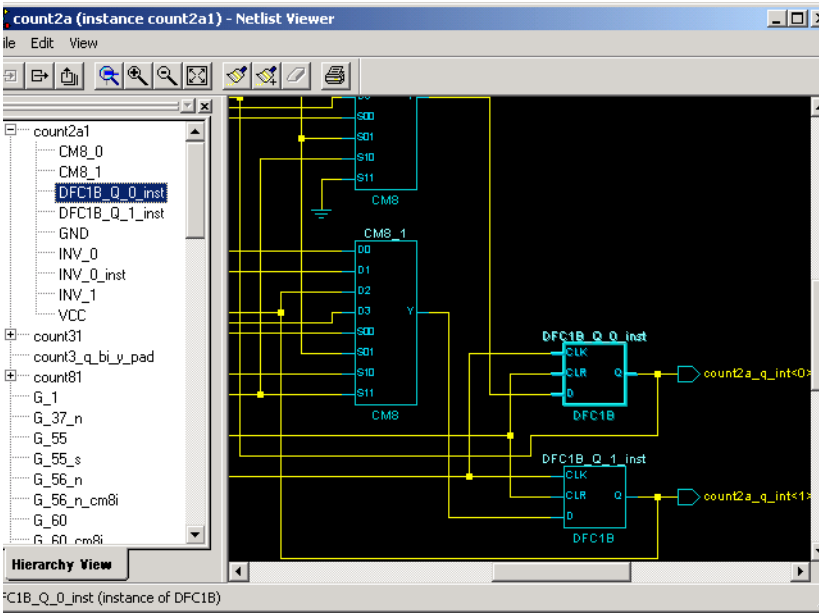



*Figure 2-7. Hierarchy View Window*

# Highlighting Objects

Highlight objects or groups of objects for easy reference. Highlighted objects are designated by the color red.

## To highlight an object:

1. **Select the object in the Netlist Viewer.**

2. **From the Edit menu, click *Highlight* or click the *Highlight* button in the toolbar.** The object changes from yellow or blue, to red, as shown in Figure 2-8.

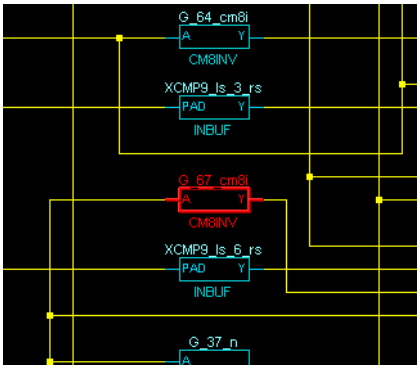



*Figure 2-8. Highlighted Object*

### To highlight a group of objects:

1. **Select the object in the Netlist Viewer.**
2. **From the Edit menu, click *Highlight* or click the *Highlight* button in the toolbar.** The object changes from blue or yellow to red.
3. **Select another object to add to the group.** Select multiple objects by holding down the SHIFT key while selecting.
4. **From the Edit menu, click *Highlight Append* or click the *Highlight Append* toolbar button.** Continue selecting and adding

objects you want marked as a group. This can be useful for tracing a net,as shown in Figure 2-9.

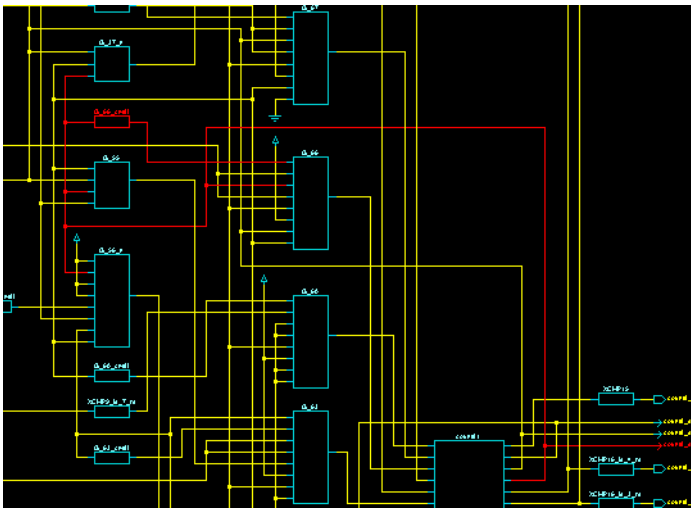


*Figure 2-9. Highlighting Groups*

### To un-highlight an object or group of objects:

1. **Select the object, or the group of objects.** To select a group, hold the Shift key while selecting objects with your mouse.
2. **From Edit menu, click *Un-highlight*, or click the Un-highlight toolbar button.**

### To un-highlight all objects:

1. **From the Edit menu, click *Clear Highlight*, or click the Clear Highlight toolbar button.** All marked objects in the current level are unmarked.

# Searching

Searching for objects can shorten your debug time. Use the Search window to search for instances, nets, and ports.

## To search for an instance, net or port:

1. **From the View menu, click *Search Tool.*** The Search Window opens,as shown in Figure 2-10.

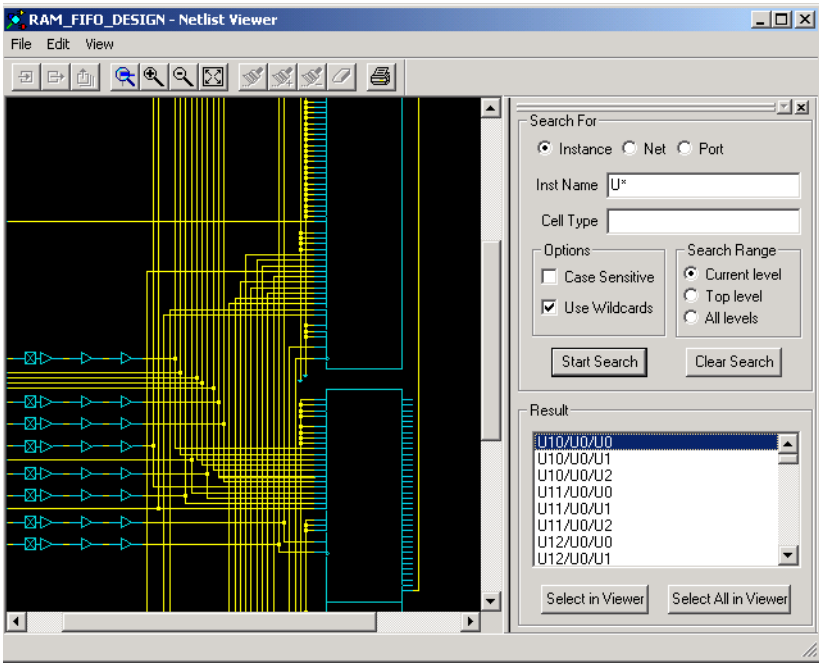



*Figure 2-10. Searching*

2. **Select Instance, Net, or Port in the Search for area.**

   Type the text you are looking for in the Name area (Inst Name, Port Name, or Net Name depending upon which radio button is selected) and/or Cell Type fields. Cell Type is only available for instance searches. When searching for instances, Inst Name or Cell Type can be blank, but not both.

These fields accept regular expressions. Wildcards in regular expression include:

- ? matches any single character
- * matches any string
- [ ] matches any single character among those listed between brackets
- [A-Z] matches any single character in range A-Z
- [Z-A] matches any single character in range A-Z
- / is the level-bordering symbol. "A/B" designates "object B, which is part of instance A". Note that the level-bordering symbol cannot be put between brackets in a regular expression.

3. **Select Search Options in the Options area.** Click the Wildcards radio button if you want to search using wildcards. Click Case Sensitive if you want the search to only return items with the exact characters specified.
4. **Define Search Range.** In the Search Range area, select your search parameters. Select top level, current level, or all levels.
5. **Click *Start Search*.** The located objects, if any, appear in the Result window.
6. **Locate objects in the Schematic View.** Selecting one or several objects in the Result window and clicking *Select In Viewer* selects the objects in the Schematic View. Simply clicking *Select All In Viewer* selects all found objects in the Schematic View.

## Using Netlist Viewer with Timer

Use the Netlist Viewer with Timer to view and trace entire paths. For more detailed information about Timer, please refer to the *Timer User's Guide*.

## Tracing Timing Paths

### To trace paths using the Netlist Viewer and Timer:

1. **Start Netlist Viewer.** Click on *Netlist Viewer* in Designer's Design Flow window.


Note: Your design must be compiled in order to start Netlist Viewer. If it isn't compiled, Designer prompts you to do so.

Netlist Viewer starts, displaying your netlist as shown in Figure 2-11.

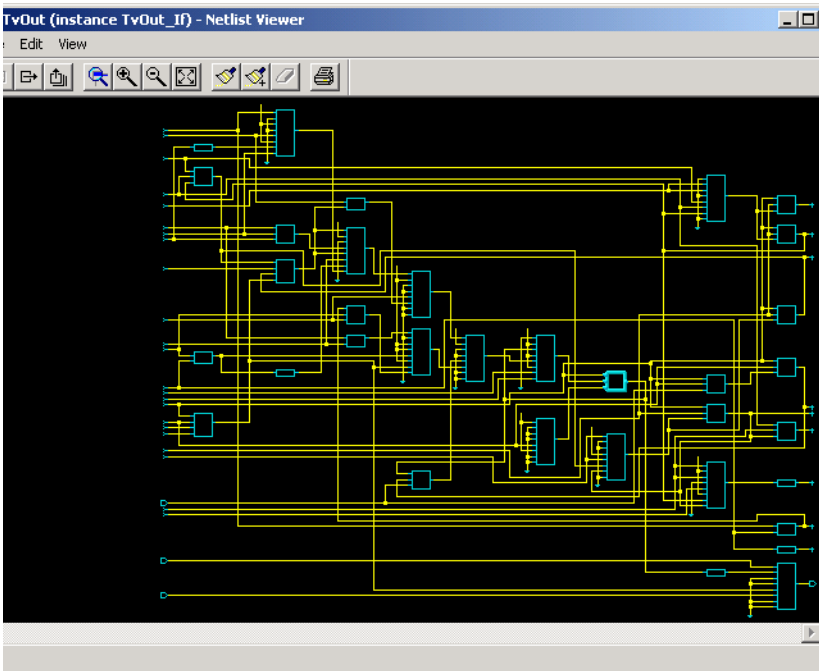



*Figure 2-11. Netlist Viewer*

2. **Start Timer.** Click on *Timer* in Designer's Design Flow window.


Timer starts,as shown in Figure 2-12

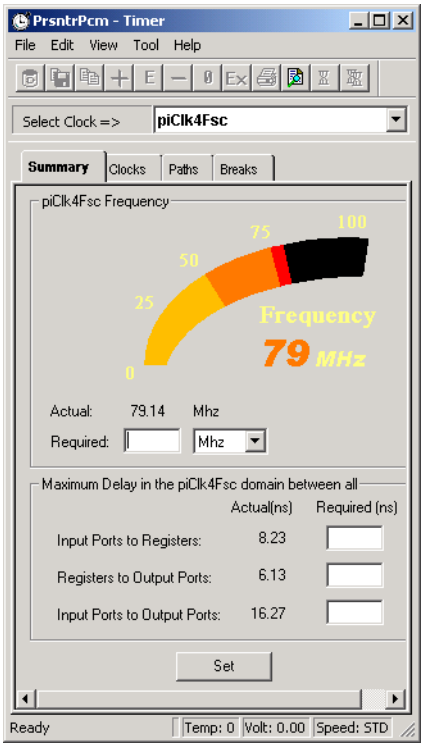



*Figure 2-12. Timer Starts*

3. **Click the Timer *Paths* tab.** The Paths tab is displayed, as shown in Figure 2-13.

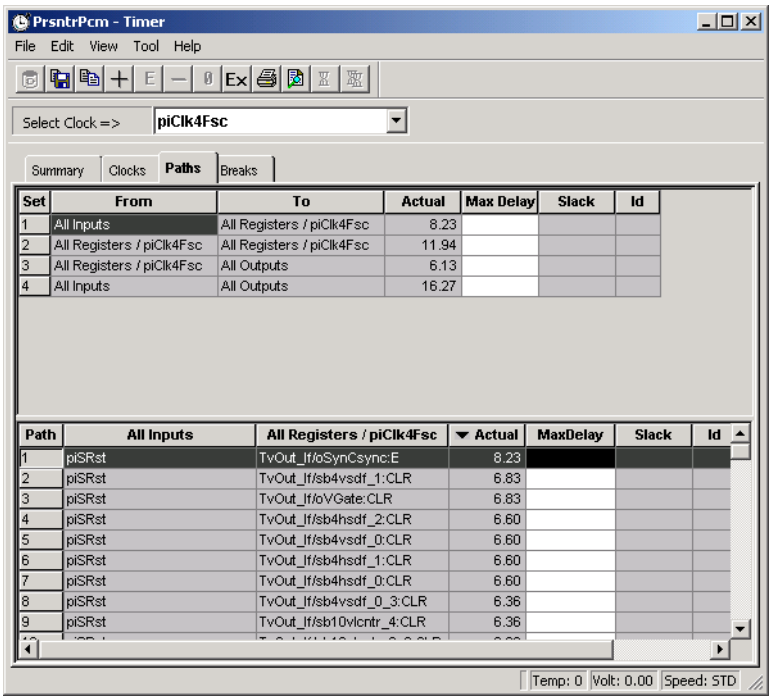



*Figure 2-13. Paths Tab*

4. **Select a Path set in the path set grid.** Paths within that set are displayed below in the path grid.
5. **Select the path you wish to expand in the lower path set grid.**

6. **Expand the path by double-clicking on the path, or in the Edit menu, click *Expand Path*. the Expanded Paths window opens, as shown in Figure 2-14.**

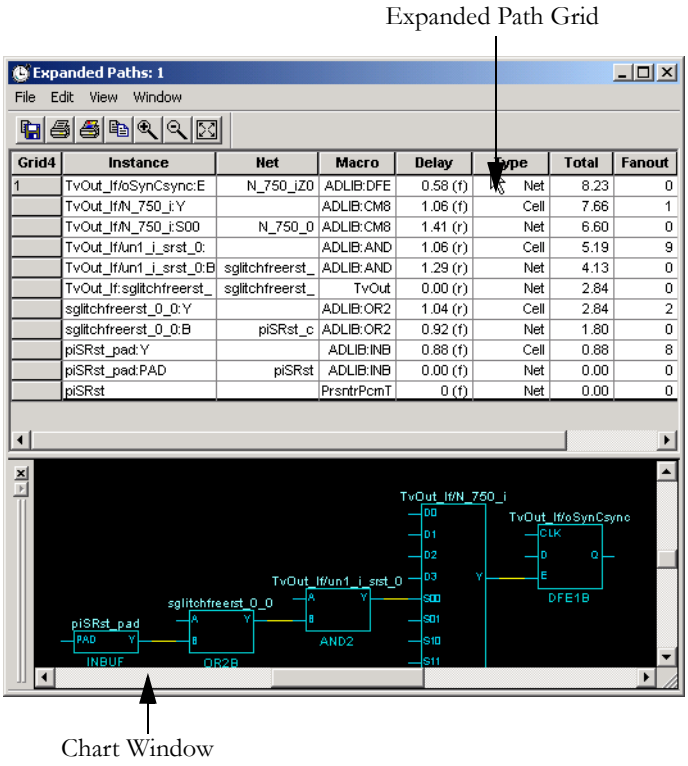



*Figure 2-14. Expanded Paths*

The Expanded Paths window displays the path in the Expanded Paths Grid and a graphical representation of the path in the Chart Window.

7. **Select an instance in the Expanded Paths grid or in the Chart Window.** The instance is highlighted in the Netlist Viewer, as shown in Figure 2-15.

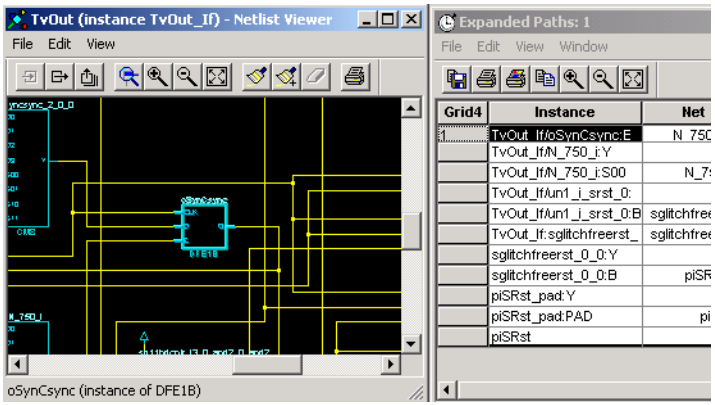



*Figure 2-15. Instance in Timer is Highlighted in Netlist Viewer*

8. **Select the first register in the timer path and locate it in the Netlist Viewer. Follow the entire path in the Netlist Viewer.** To mark the path for easy identification and reference, see "Highlighting Groups" on page 26.

# Using Netlist Viewer with ChipEdit

If both the Netlist Viewer and ChipEdit are open, items selected in either tool are selected and highlighted in the other. For more details about ChipEdit, please refer to the *ChipEdit User's Guide*.

## To use Netlist Viewer with ChipEdit:

1. **Start Netlist Viewer.** Click on *Netlist Viewer* in Designer's Design Flow window.

Netlist Viewer starts, displaying your netlist, as shown in Figure 2-16.

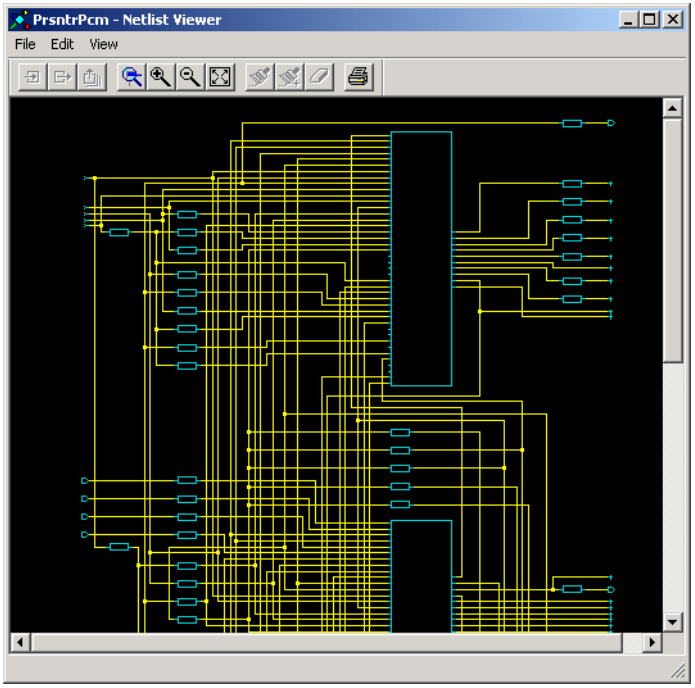



*Figure 2-16. Netlist Viewer Starts*

2. **Start ChipEdit.** From Designer's Flow Window, click *ChipEdit*.

ChipEdit opens in a separate window displaying the logic and I/O modules on the device.as shown in Figure 2-17.

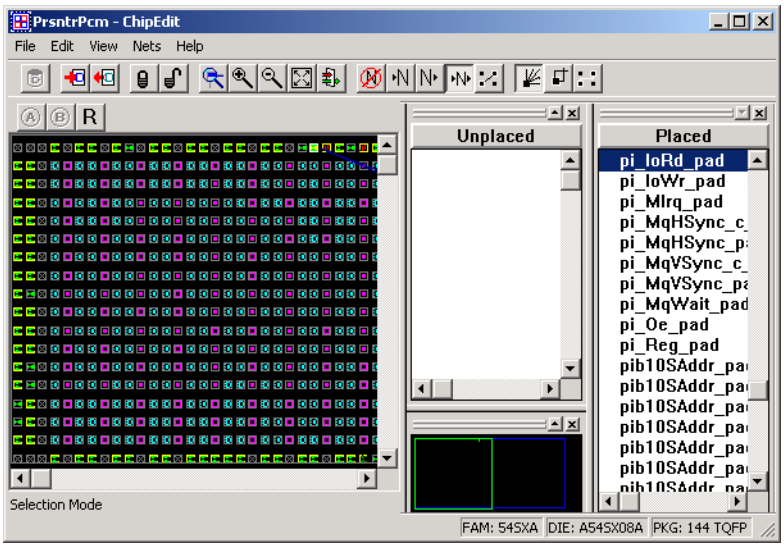



*Figure 2-17. ChipEdit Window*

3. **Select a macro or instance in the ChipEdit or Netlist Viewer.**
   The item is selected in the other tool,

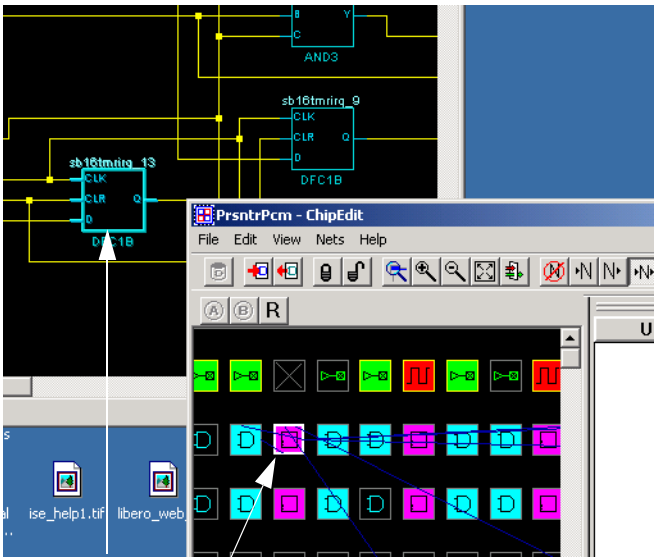



*Figure 2-18. Item is Selected in Both ChipEdit and Netlist Viewer*

# 3

# Netlist Viewer Examples

The examples in this chapter illustrate common applications for the Netlist Viewer.

## Debugging Simulation Results

The Netlist Viewer is useful for debugging the netlist when simulation results are confusing or unacceptable.

In this example, an unknown (red) signal appears as an output when simulation is performed, as shown in Figure 3-1.

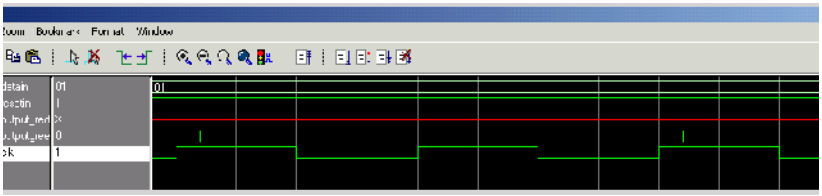


*Figure 3-1. Investigating Signal Output*

In most cases, this occurs when the output of a flip flop is being fedback into the input without a reset, prset, or clear input. The Netlist Viewer can help you verify that such flip flop configuration exist in the design.

### Locating and viewing the flip flops:

1. **Start the Netlist Viewer.** Click *Netlist Viewer* in the Design Flow window. The Netlist Viewer starts and displays your netlist.

2. **Zoom to locate the flip flops, as shown in Figure 3-2.**

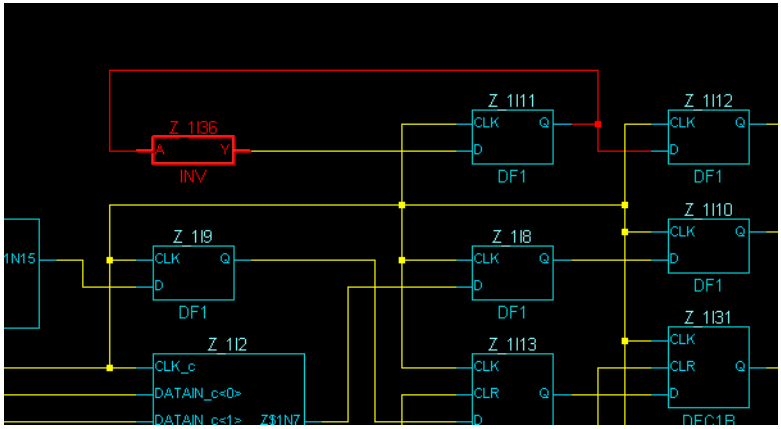



*Figure 3-2. Flip Flop Feedback*

# Identifying Paths

In this example, the Netlist Viewer is used with Timer to identify the inputs of combinational gates. For more detailed information about Timer, refer to the *Timer User's Guide*.

### To identify these paths:

1. **From Designer, start Netlist Viewer.** Click *Netlist Viewer* in the Design Flow window. The Netlist Viewer starts and displays your netlist,as shown in Figure 3-3.

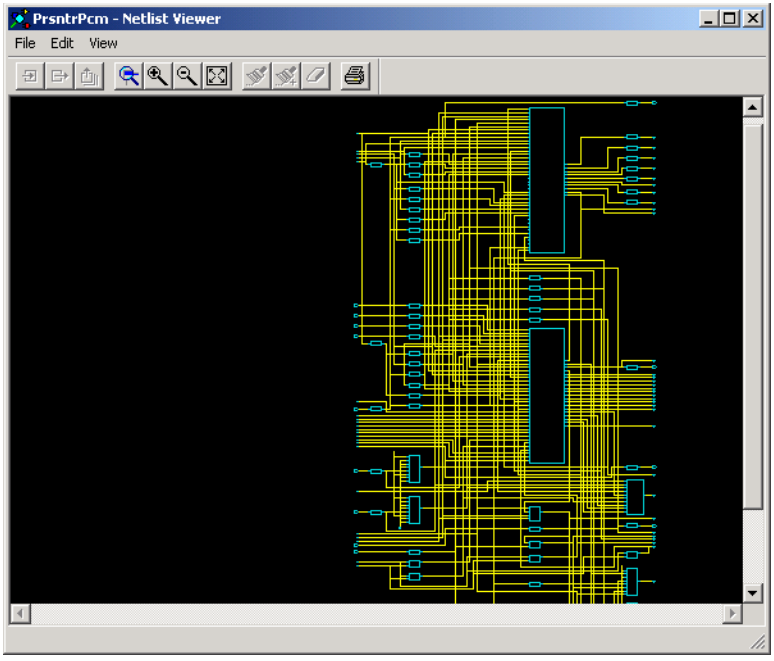



*Figure 3-3. Starting Netlist Viewer*

2. **From Designer, start Timer.** Click *Timer* in the Designer Flow Window. Timer starts, as shown in Figure 3-4

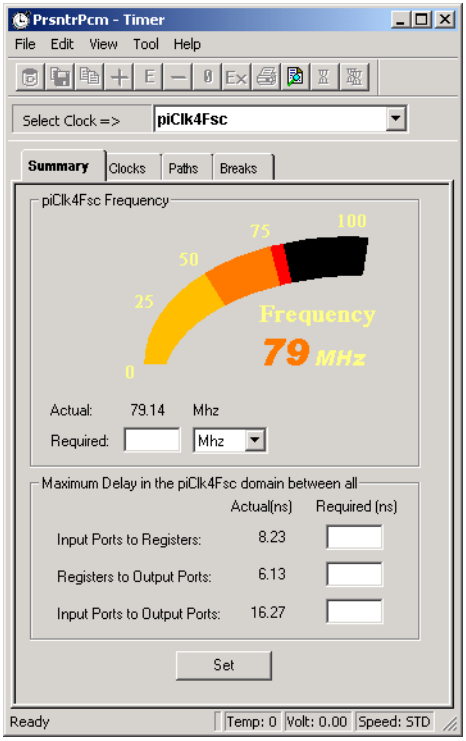



*Figure 3-4. Starting Timer*

3. **In Timer, click the *Paths* tab, as shown in Figure 3-5.**

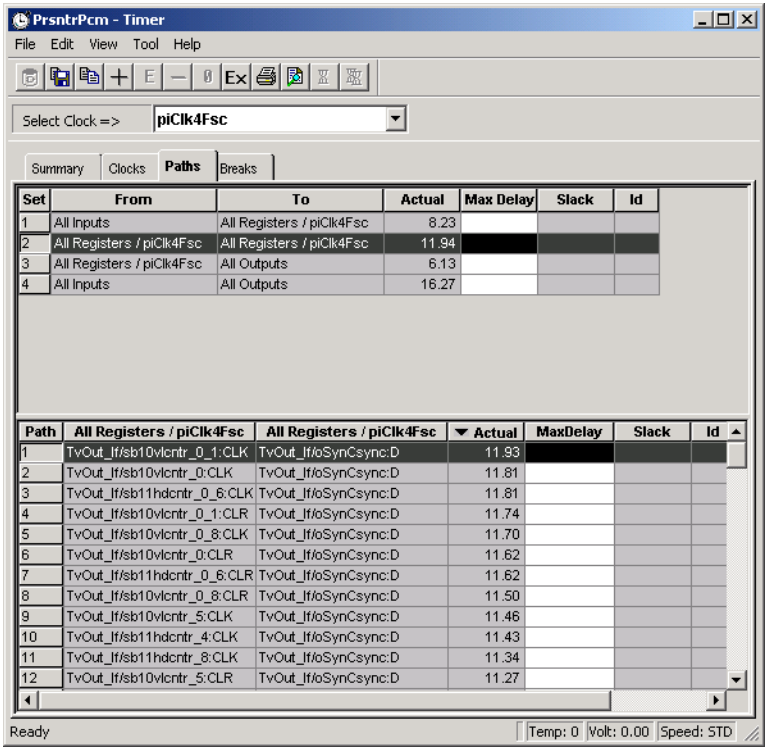



*Figure 3-5. Timer's Paths Tab*

The paths tab displays timing analysis information for four categories of paths, known as "sets," in the upper grid. When a set is selected in this upper grid, the paths within that set are displayed in the lower grid.

4. **Select a Path Set in the upper path set grid.** The paths within that set are displayed in the lower grid.

5. **Expand a path.** Double-click a path in the lower paths grid. The Expanded Paths window opens, as shown in Figure 3-6.

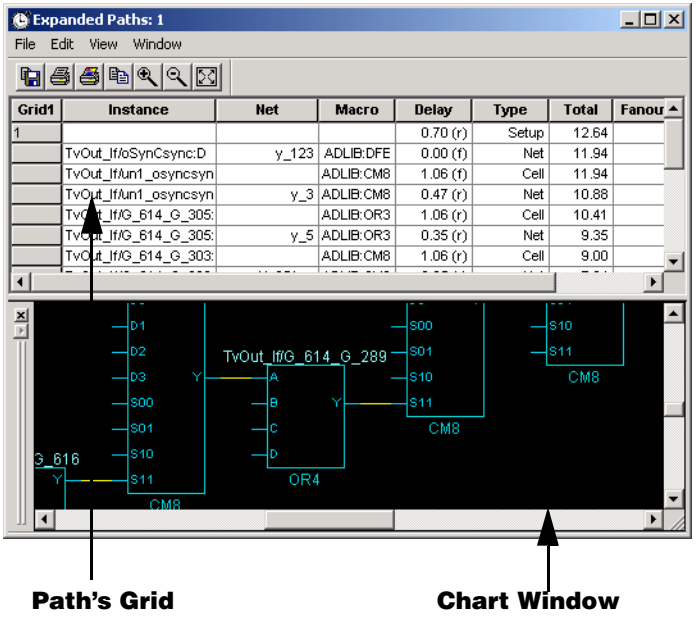



*Figure 3-6. Expanding the Path*

The Expanded Paths window displays a path in the Expanded Paths Grid and a graphical representation of the path in the Chart Window.

Notice that the inputs of combinational gates are not shown in the Chart Window, as shown in Figure 3-7.

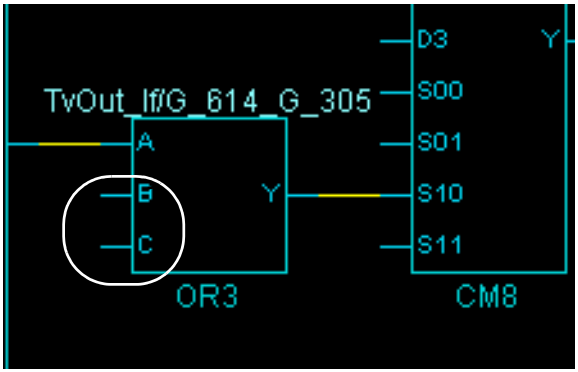



*Figure 3-7. Combinational Gates in Timer's Expanded Paths Window*

It's useful to know where these paths come from because it might indicate a false path, which never happens during the design and can affect the timing report. It's very useful to know the interaction of other inputs to these macros with the indicated path because it helps in defining the appropriate paths and timing reports.

6. **Select the Macro in the Chart window.** The macro is located and selected in the Netlist Viewer, as shown in Figure 3-8.

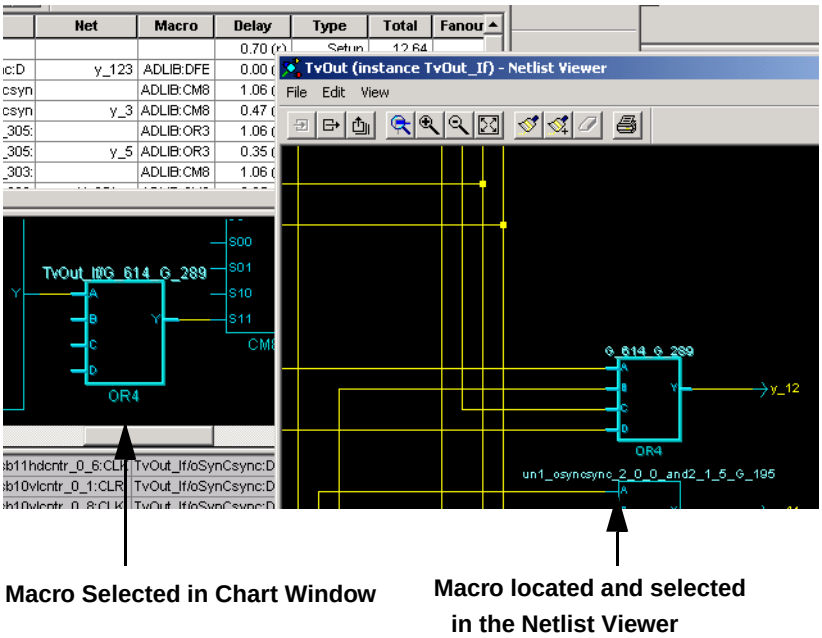



*Figure 3-8. Selected Macro is Located and Selected in the Netlist Viewer*

7. **Using the Netlist Viewer, you can now track the other inputs into the path.**

# Viewing Buffers

The Netlist Viewer is useful to see buffers inserted by your synthesis tool due to the high fanout number of some signals.

### To view inserted buffers:

1. **Start Netlist Viewer.** Click *Netlist Viewer* in the Design Flow window. The Netlist Viewer starts and displays your netlist,as shown in Figure 3-9.

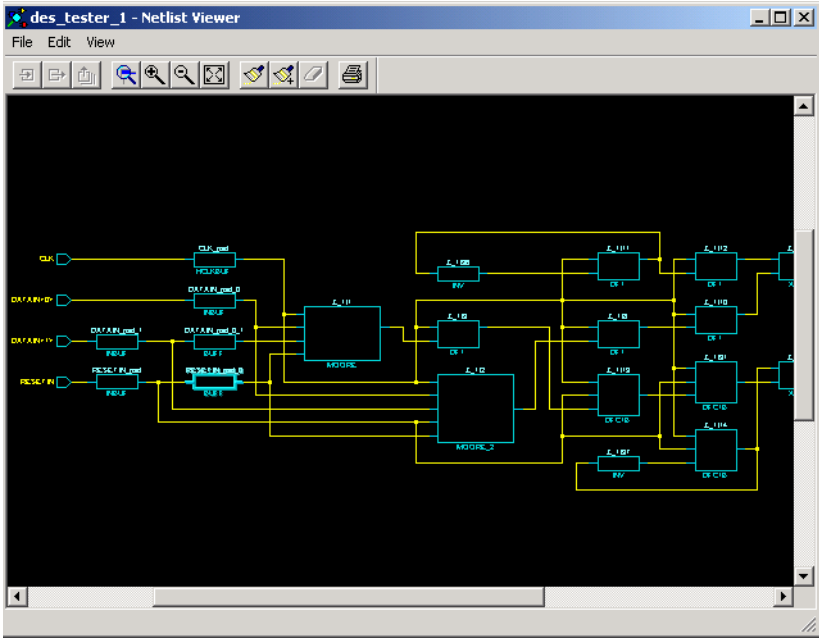



*Figure 3-9. Netlist Viewer Starts*

In this example, since the fanout of DATAIN and RESET inputs of the design exceeds the specified value in the synthesis tool, Synplicity inserts 2 buffers in

their path to reduce the number of fanout for these signals, as shown in Figure 3-10.

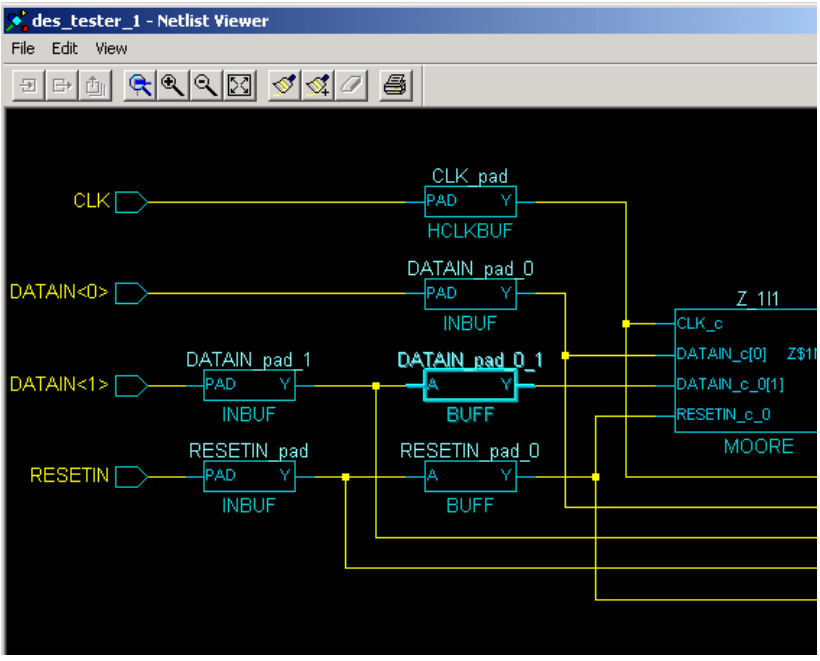



*Figure 3-10. Inserted Buffers*

2. **Using Netlist Viewer, you can track these inserted buffers.**
3. **(Optional) Examine the timing effect of these buffers using Timer.** Click *Timer* in Designer's Design Flow Window.

# A

# Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

## Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

## Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
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## Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

# Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (http://www.actel.com/guru/). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site.

# Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

# Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

## Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

## Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

***(408) 522-4460***
***(800) 262-1060***

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Please see our list of Worldwide Sales Offices.

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