Power Requirements: Actel A54SX08 vs. Altera CPLDs

Introduction

FPGAs have traditionally been perceived as inferior in performance to CPLDs. Actel's high-performance antifuse SX family, however, offers both superior speed and reduced power in a single device. To see how well the SX family compares against a CPLD, Actel performed a laboratory comparison between the Actel A54SX08 FPGA and the Altera EPM7256A CPLD using four typical designs selected to highlight worst-case conditions in various scenarios.

Device Data

The Altera EPM7256A CPLD was selected for comparison to the Actel A54SX08 FPGA because both feature a similar capacity (Table 1). Although the SX device is architecturally an FPGA, it can achieve the same functionality as a MAX 7000A CPLD.

Table 1 • *Device Comparison*

	Altera EPM7256A	Actel A54SX08
Number of Logic Elements	256	768
Dedicated Flip-Flops	256	256

Altera's MAX 7000A CPLDs have a power-saving mode that supports power reduction on a per macrocell basis. The macrocells running in low-power mode incur an additional delay of at least 10 ns. This comparison used both high-speed (turbo) mode and low-power (nonturbo) modes.

The speed grades considered were the fastest available at the time of this experiment. The EPM7256A fastest speed grade was –7, and the A54SX08 fastest speed grade was –2. Faster devices may now be available for both devices.

In the Laboratory

Semiconductor power requirements depend on a multitude of factors, including power supply voltage, technology, operating performance, and switching activity. Mathematical models are useful tools for estimating power, but they cannot replace measured data. Most power models are approximations, simplified for general usability. Although these models provide an adequate guide for power requirements, the best way to determine the actual power performance is through physical device measurements.

Four designs were generated and programmed into the devices. A shift-register design demonstrated sequential logic functionality; a multiplier design used combinatorial logic; a counter design used a mix of sequential and combinatorial logic; and a clock-tree design compared the clock functionalities.

Each device used the same design. All four designs were "self-exciting" with the global clock as their only input. Each design also used a small number of outputs to ensure valid circuit operation.

A socket module for each device was constructed for testing purposes. A terminated connection, consisting of a coaxial cable connected as closely as possible to the clock-input pin to reduce the noise level of the setup, routed the input to the device.

A Hewlett-Packard E3615A Digital Power Supply driving 3.3V powered all devices. A LeCroy 9210 300MHz Function Generator with a maximum frequency of 300MHz drove the clock. A Fluke 8050A Digital Multimeter was used to measure power in terms of device power-supply current (I_{cc}), which was then converted into power dissipation (measured in Watts).

Power Comparison Analysis

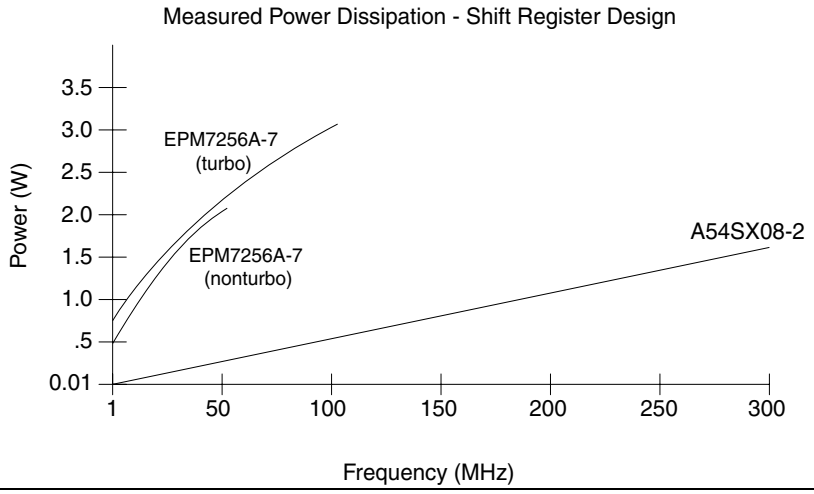

Figure 1 • *Power Requirements - Shift-Register Design*

Shift Register

The 256-bit shift-register design had the highest power dissipation design measurements in the suite. It required 100% of the flip-flops to switch on every clock pulse, providing an indication of absolute worst-case power dissipation for each device.

The turbo bit in the Altera EPM7256A did not significantly alter the power consumption of the shift-register design. This may be because every logic element was switching on each clock pulse. The turbo bit is not effective at reducing power in designs with multiple bits.

The Actel A54SX08 device consumed 85% less power at 50MHz than the Altera EPM7256A device (Figure 1). The EPM7256A reached a maximum operating frequency of 110MHz in this design. The power requirements of the A54SX08 operating at 300MHz are approximately equal to the requirements of the EPM7256A operating at 30MHz.

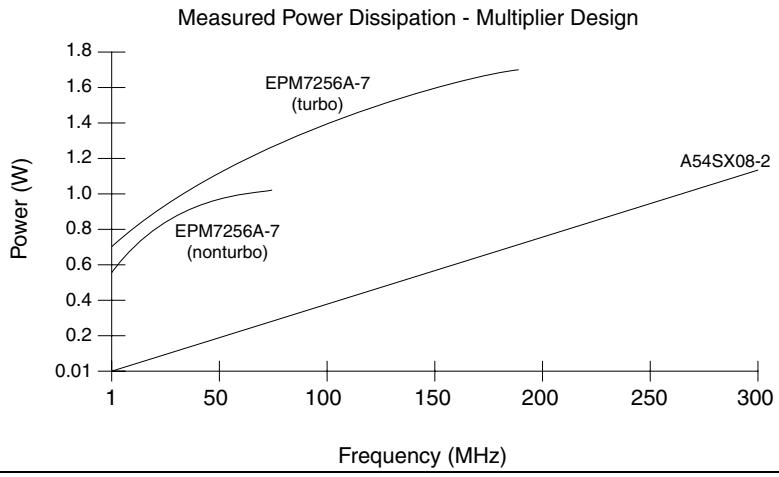

Figure 2 • *Power Requirements - Multiplier Design*

Multiplier Design

The 8x8 multiplier design provided a comparison between the two devices implementing combinatorial logic.

The disabling of the turbo bit in the Altera EPM7256A device resulted in slightly lower power than with the turbo bit enabled.

The A54SX08 device consumed approximately 80% less power than the EPM7256A at 50MHz in high-speed mode and 78% less power than the EPM7256A at 50MHz in low-power mode. At its maximum operating frequency, the EPM7256A consumed as much as 2.5 times more power than the A54SX08 device.

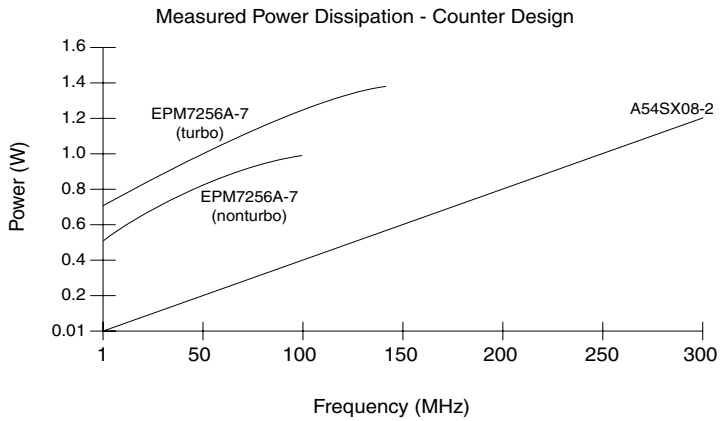

Figure 3 • Power Requirements - Counter Design

Counter Design

This design used multiple instances of an 8-bit counter and provided an excellent comparison of the power requirements of the devices implementing both sequential and combinatorial logic.

The disabling of the turbo bit in the EPM7256A resulted in a drop in power when compared to the device with the turbo bit enabled. This is because the majority of bits in a counter design do not change often enough to affect the results.

The A54SX08 consumed 80% less power than the EPM7256A at 50MHz in high-speed mode and 75% less power in low-power mode. The EPM7256A in high-speed mode reached a maximum operating frequency of 140MHz. At this frequency the EPM7256A consumed as much as 2.5 times more power than the A54SX08.

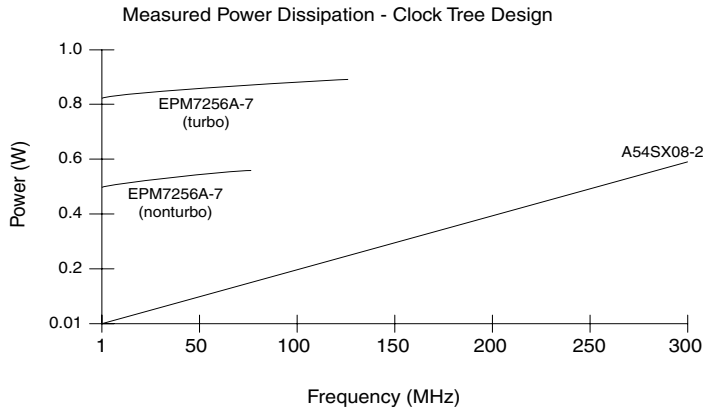

Figure 4 • Power Requirements - Clock-Tree Design

Clock-Tree Design

The clock-tree design compared the power efficiency of the global clock-tree in each device. Although the A54SX08 has a physically larger clock-tree, it consumed considerably less power than the EPM7256A, due in part to the much higher standby current of the EPM7256A.

The A54SX08 device consumed 85% less power than the EPM7256A device at 50MHz in high-speed mode and 80% less power in low-power mode. The EPM7256A in high-speed mode ceased to function at an operating frequency of 120MHz, where it consumed approximately 3.5 times the power of the A54SX08.

Conclusions

The A54SX08 FPGA was able to achieve both higher performance and lower power than the EPM7256A CPLD. Based on the suite of four designs tested, the Actel A54SX08 consumed an average of 80% less power than the EPM7256A operating in high-speed mode. At the same time, the A54SX08 also operated at frequencies well above the maximum operating frequency of the EPM7256A. Only the hardware limitations of the test equipment restrict the maximum operating frequency of 300MHz for the A54SX08.

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