54SX Family FPGAs
RadTolerant and HiRel

Features

RadTolerant 54SX Family

- Tested Total Ionizing Dose (TID) Survivability Level
- Devices Available from Tested Lots
- Radiation Performance to 100K Rads
- Up to 160 MHz On-Chip Performance
- Offered as E-Flow (Actel Space Level Flow) and Class B

HiRel 54SX Family

- Fastest HiRel FPGA Family Available
- Up to 240 MHz On-Chip Performance
- Low Cost Prototyping Vehicle for RadTolerant Devices
- Offered as Commercial or Military Temperature Tested and Class B

High Density Devices

- 16,000 and 32,000 Available Logic Gates
- Up to 225 User I/Os
- Up to 1,080 Dedicated Flip-Flops

Easy Logic Integration

- Non-Volatile, User Programmable
- Highly Predictable Performance with 100% Automatic Place and Route
- 100% Resource Utilization with 100% Pin Locking
- Mixed Voltage Support—3.3V Operation with 5.0V Input Tolerance
- JTAG Boundary Scan Testing in Compliance with IEEE Standard 1149.1
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Permanently Programmed for Instantaneous Operation on Power-Up
- Unique In-System Diagnostic and Debug Facility with Silicon Explorer
- Actel Designer Series Design Tools, Supported by Cadence, Exemplar, Mentor Graphics, Model Tech, Synopsys, Synplicity, and Viewlogic Design Entry and Simulation Tools

General Description

The New SX Family of FPGAs

Actel's SX Family of FPGAs features a revolutionary new sea-of-modules architecture that delivers next-generation device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further speed time-to-market for performance-intensive applications.

SX Product Profile

	RT54SX16	A54SX16	RT54SX32	A54SX32
Gate Capacity	16,000	16,000	32,000	32,000
Logic Modules	1,452	1,452	2,880	2,880
Register Cells	528	528	1,080	1,080
Combinatorial Cells	924	924	1,800	1,800
User I/Os (Maximum)	177	176	224	225
JTAG	Yes	Yes	Yes	Yes
Packages (by pin count)				
CQFP	208, 256	208, 256	208, 256	208, 256

Actel's RadTolerant (RT) and HiRel versions of the SX Family of FPGAs offer all of these advantages for applications such as commercial and military satellites, deep space probes, and all types of military and high reliability equipment.

The RT and HiRel versions are fully pin compatible allowing designs to migrate across different applications that may or may not have radiation requirements. Also the HiRel devices can be used as a low cost prototyping tool for RT designs.

The programmable architecture of these devices offer high performance, design flexibility and fast and inexpensive prototyping—all without the expense of test vectors, NRE charges, long lead times and schedule and cost penalties for design modifications required by ASIC devices.

Device Description

The RT54SX16 and A54SX16 devices have 16,000 available gates and up to 177 I/Os. The RT54SX32 and A54SX32 have 32,000 available gates and up to 225 I/Os. All of these devices support JTAG boundary scan testability.

All of these devices are available in Ceramic Quad Flat Pack (CQFP) packaging, with 208-pin and 256-pin versions. The 256-pin version offers the user the highest I/O capability, while the 208-pin version offers pin compatibility with the commercial Plastic Quad Flat Pack (PQFP-208). This compatibility allows the user to prototype using the very low cost plastic package and then switch to the ceramic package for production. For more information on plastic packages, please refer to the SX Series FPGAs data sheet, located on the Actel web site at:

http://www.actel.com/products/devices/datasheets.html.

The A54SX16 and A54SX32 are manufactured using a 0.35u technology at the Chartered Semiconductor facility in Singapore. These devices offer the highest speed performance available in FPGAs today.

The RT54SX16 and RT54SX32 are manufactured using a 0.6u technology at the Matsushita (MEC) facility in Japan. These devices offer levels of radiation survivability far in excess of typical CMOS devices.

Radiation Survivability

Total dose results are summarized in two ways. First, the maximum total dose level that is reached when the parts fail to meet a device specification but remain functional. For Actel FPGAs, the parameter that exceeds the specification first is ICC, the standby supply current. Second, the maximum total dose that is reached prior to the functional failure of the device.

The RT devices have varying total dose radiation survivability. The ability of these devices to survive radiation effects is both device and lot dependent. The customer must evaluate and determine the applicability of these devices to their specific design and environmental requirements.

Typical results for the RT devices have shown from 60 to 100 Krads (Si) for standby ICC, and up to 240 Krads for functional failure.

Actel will provide total dose radiation testing on each lot that is available for sale. Actel will provide these reports on our website or you can contact your local sales representative to receive a copy. We will also provide a listing of available lots and devices. These results are only provided for reference and for customer information.

A summary of the radiation performance of Actel products ("Radiation Performance of Actel Products") can be found on the Actel Web site at

http://www.actel.com/products/devices/radhard/radperf.pdf

This summary will also show SEU and SEL testing that has been performed.

Disclaimer

All radiation performance information is provided for information purposes only and is not guaranteed. The total dose effects are lot-dependent, and Actel does not warrant that future devices will continue to exhibit similar radiation characteristics. In addition, actual performance can vary widely due to a variety of factors, including but not limited to, characteristics of the orbit, radiation environment, proximity to satellite exterior, amount of inherent shielding from other sources within the satellite and actual bare die variations. For these reasons, Actel does not warrant any level of radiation survivability, and it is solely the responsibility of the customer to determine whether the device will meet the requirements of the specific design.

Design Tool Support

As with all Actel FPGAs, these devices are fully supported by Actel's Designer Series development tools, which include:

- DirectTime for automated, timing-driven place and route;
- ACTgen for fast development using a wide range of macro functions; and
- ACTmap for logic synthesis.

Designer Series supports industry-leading VHDL- and Verilog-based design tools, including synthesis tools from industry leaders such as Exemplar Logic, Synplicity, and Synopsys.[1]

1. Designer Series also supports design entry and simulation tools from Cadence, Mentor Graphics, and Viewlogic.

In addition, these devices are supported by Actel's new Silicon Explorer diagnostic and debugging tool kit. Silicon Explorer dramatically reduces verification time from several hours per cycle to a few seconds by enabling real-time, in-circuit debugging. Silicon Explorer includes:

- Probe Pilot, a high-speed signal acquisition and control tool that samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Probe Pilot features 18 probing channels and connects to the user's PC via a standard serial port connection.
- Diagnostic software, which turns the PC into a fully-featured, 100 MHz logic analyzer for easy graphical analysis of waveforms.

Silicon Explorer probes 100 percent of the device circuitry using Probe Pilot's powerful, 18-channel signal acquisition capability. Individual bugs are then isolated and passed to the user interface, providing the user with complete waveform data.

Fast and Flexible New Architecture

Actel's SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. Optimal use of the silicon is made by locating the routing and interconnect resources in the metal layers above the logic modules, enabling the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules") which reduces the distance signals have to travel between logic modules.

To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (typically 90% of connections use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100% pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with a minimum of effort.

Further complementing the SX's flexible routing structure, a hard-wired, constantly-loaded clock network has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SX devices have easy-to-use I/O cells which do not require HDL instantiation, facilitating design re-use and reducing design and debugging time.

Ordering Information

RT54SX32 – 1 CQ 256 B

- **B** — Application (Temperature Range)
  - Blank = Commercial (0 to +70°C)
  - M = Military (–55 to +125°C)
  - B = MIL-STD-883
  - E = E-Flow (Actel Space Level Flow)
- **256** — Package Lead Count
- **CQ** — Package Type
  - CQ = Ceramic Quad Flat Pack
- **1** — Speed Grade
  - Blank = Standard Speed
  - –1 = Approximately 15% Faster than Standard
- **RT54SX32** — Part Number
  - A54SX16 = 16,000 Gates
  - A54SX32 = 32,000 Gates
  - RT54SX16 = 16,000 Gates—RadTolerant
  - RT54SX32 = 32,000 Gates—Rad Tolerant

Product Plan

	Speed Grade		Application			
	Std	–1*	C	M	B	E
RT54SX16 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	P
A54SX16 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	—
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	—
RT54SX32 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	P
A54SX32 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	—
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P	—

Consult your local Actel sales representative for product availability.

Applications: *C = Commercial* *M = Military* *B = MIL-STD-883* *E = E-flow (Actel Space Level Flow)*

Availability: ✔ = *Available* *P = Planned* — = *Not Planned*

** Speed Grade: –1 = Approx. 15% Faster than Standard*

Plastic Device Resources

Device	User I/Os	
	CQFP 208-Pin	CQFP 256-Pin
RT54SX16	171	176
A54SX16	172	177
RT54SX32	170	224
A54SX32	171	225

Package Definitions: *CQFP = Ceramic Quad Flat Pack*

(Consult your local Actel sales representative for product availability.)

Pin Description

CLKA Clock A (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

CLKB Clock B (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tri-stated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device.

PRA ActionProbe A (Output)

The ActionProbe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the ActionProbe B pin to allow real-time diagnostic output of any signal path within the device. The ActionProbe A pin can be used as a user-defined I/O when debugging has been completed.

PRB ActionProbe B (Output)

The ActionProbe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the ActionProbe A pin to allow real-time diagnostic output of any signal path within the device. The ActionProbe B pin can be used as a user-defined I/O when debugging has been completed.

TCK Test Clock (Input)

Test clock input for diagnostic probe and device programming. In flexible mode (refer to the JTAG pins functionality table), TCK becomes active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the “logic reset” state.

TDI Test Data Input (Input)

Serial input for JTAG and diagnostic probe. In flexible mode, (refer to the JTAG pins functionality table), TDI is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the “logic reset” state.

TDO Test Data Output (output)

Serial output for JTAG. In flexible mode (Refer to the JTAG pins functionality table), TDO is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the “logic reset” state.

TMS Test Mode Select (Input)

The TMS pin controls the use of JTAG pins (TCK, TDI, TDO). In flexible mode (refer to the JTAG pins functionality table), when the TMS pin is set LOW, the TCK, TDI, and TDO pins are JTAG pins. Once the JTAG pins are in JTAG mode they will remain in JTAG mode until the internal JTAG state machine reaches the “logic reset” state. At this point the JTAG pins will be released and will function as regular I/O pins. The “logic reset” state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated JTAG mode, TMS functions as specified in the IEEE 499.1 JTAG Specifications. JTAG operation is further described on page 6.

TRST Test Reset Pin (Input)

JTAG reset pin (active LOW). This pin is used to reset the JTAG state machine in “test-logic-reset” state to avoid accidental shifts into various JTAG operations due to the effects of heavy ions in a radiation environment. When this pin is tied LOW, the device is held in the ìtest-logic-resetî state and the JTAG functionality cannot be used. When this pin is tied HIGH, the JTAG function can operate. This pin should not be left floating.

V_{CCI} Supply Voltage

Supply voltage for I/Os.

V_{CCA} Supply Voltage

Supply voltage for Array.

V_{CCR} Supply Voltage

Supply voltage for input tolerance (required for internal biasing).

SX JTAG Pins Functionality Table

All SX devices feature hard-wired IEEE 1149.1 JTAG Boundary Scan Test circuitry. Figure 1 is a block diagram of the A54SX JTAG circuitry and Figure 2 shows the RT54SX JTAG circuitry.

The RT54SX devices include a TRST pin which is used to reset the JTAG state machine in “test-logic-reset” mode.

SX devices offer superior diagnostic and testing capabilities by rpoviding JTAG and probing capabilities. These functions are controlled through the special JTAG pins in conjunction with the program fuse. The functionality of each pin is described in Table 1 below.

In the dedicated JTAG mode, TCK, TDI and TDO are dedicated JTAG pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10K ohm. TMS can be pulled LOW to initiate the JTAG sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode. Regardless of which mode is chosen, tying the TRST pin LOW will disable all JTAG functionality.

Table 1 • *JTAG*

Program Fuse Blown (Dedicated JTAG Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated JTAG pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10K ohm on TMS

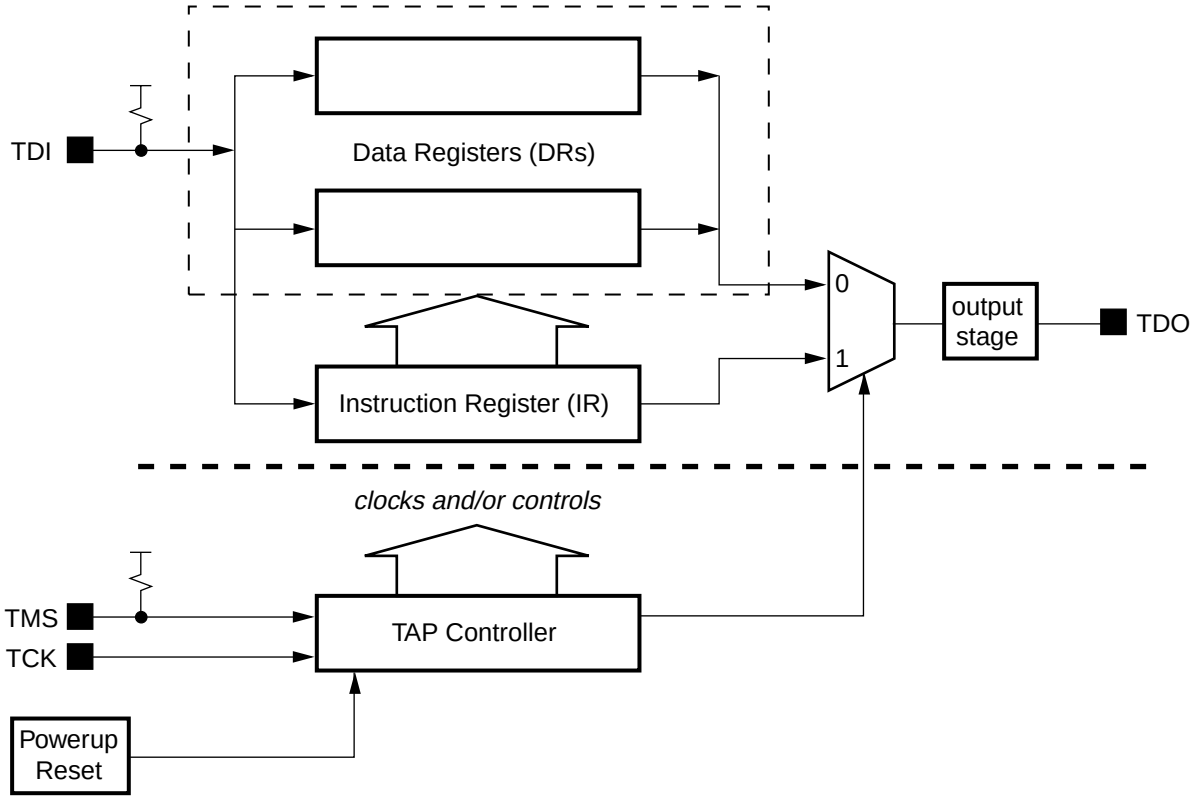


Figure 1 • *A54SX JTAG Circuitry*

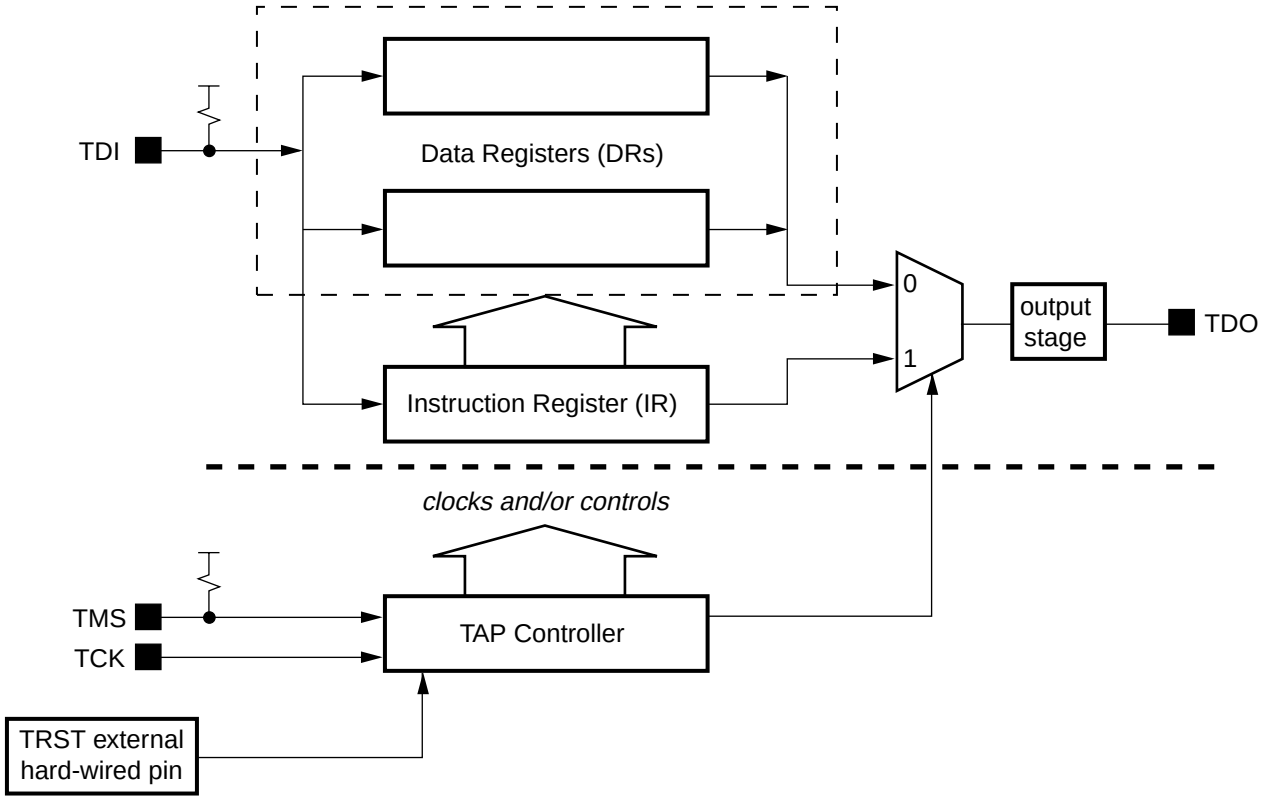


Figure 2 • *RT54SX JTAG Circutiry*

SX Family Architecture

The SX Family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

Actel's new SX Family provides much more efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (see Figure 3). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX Family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible as it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

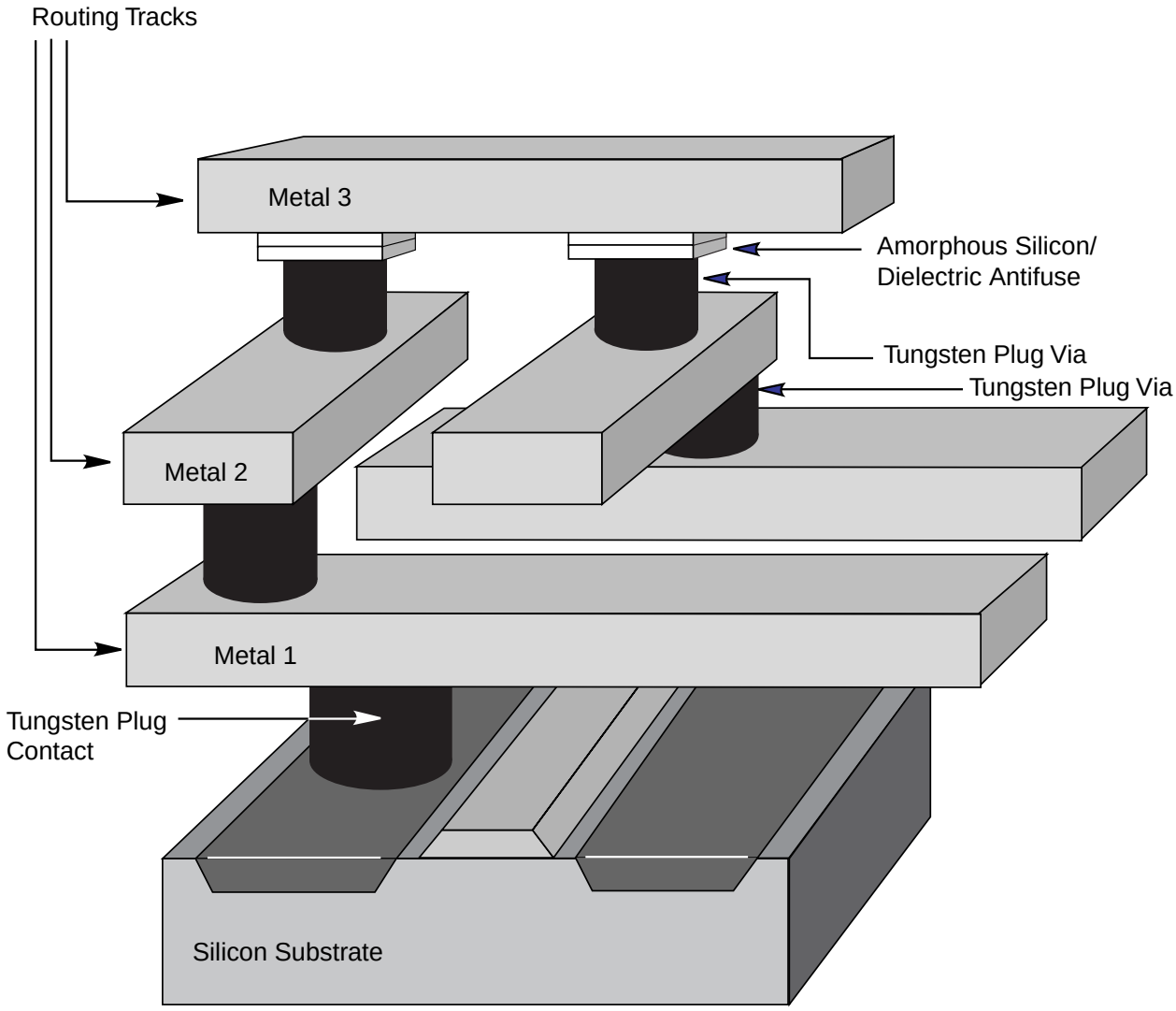


Figure 3 • *SX Family Interconnect Elements*

Logic Module Design

The SX Family architecture has been called a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing (see Figure 4). Actel provides two types of logic modules, the R-cell and the C-cell.

The R-cell (or register cell) contains a flip-flop featuring more control signals than in previous Actel architectures, including asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines). The R-cell (Figure 5) registers feature programmable clock polarity, selectable on a register-by-register basis. This provides the designer with additional flexibility while allowing mapping of synthesized functions into the SX FGPA. The clock source for the R-cell can be chosen from the hard-wired clock or the routed clock.

The C-cell (or combinatorial cell, Figure 6) implements a range of combinatorial functions up to 5-inputs. Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions which can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

Chip Architecture

The SX Family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

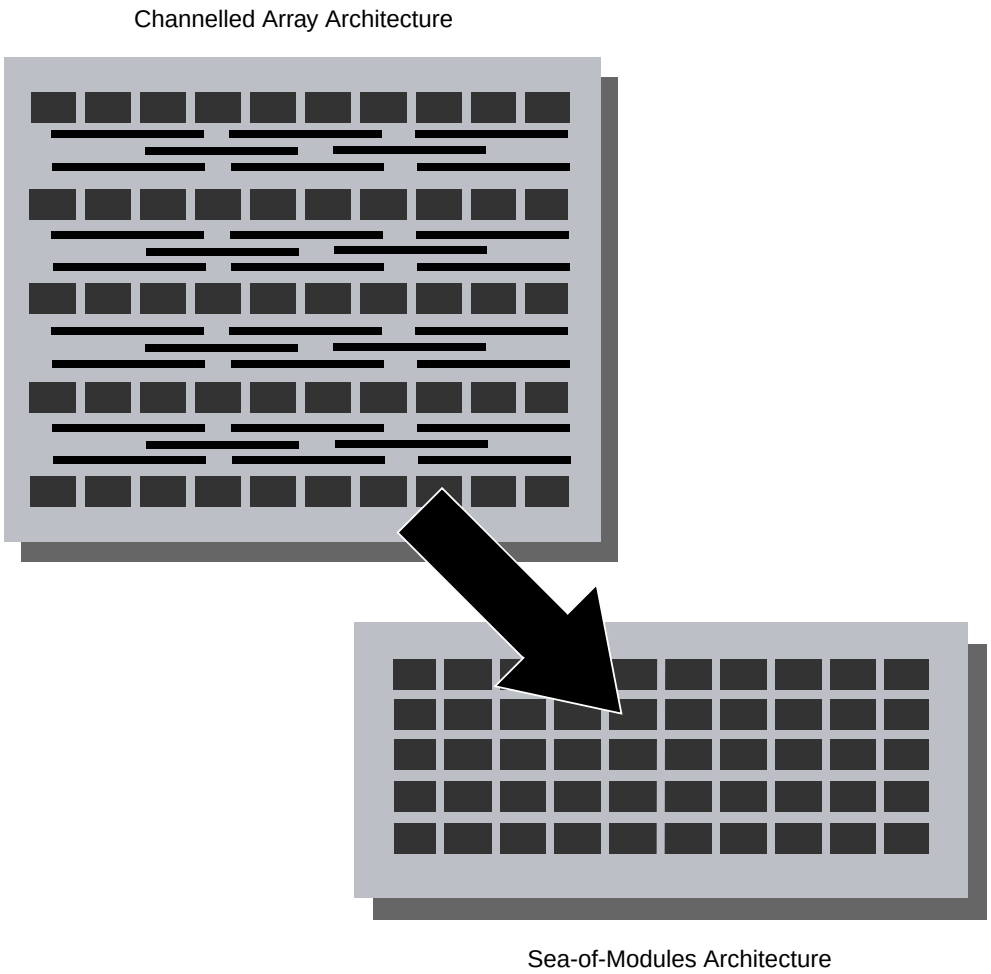


Figure 4 • *Channelled Array and Sea-of-Modules Architectures*

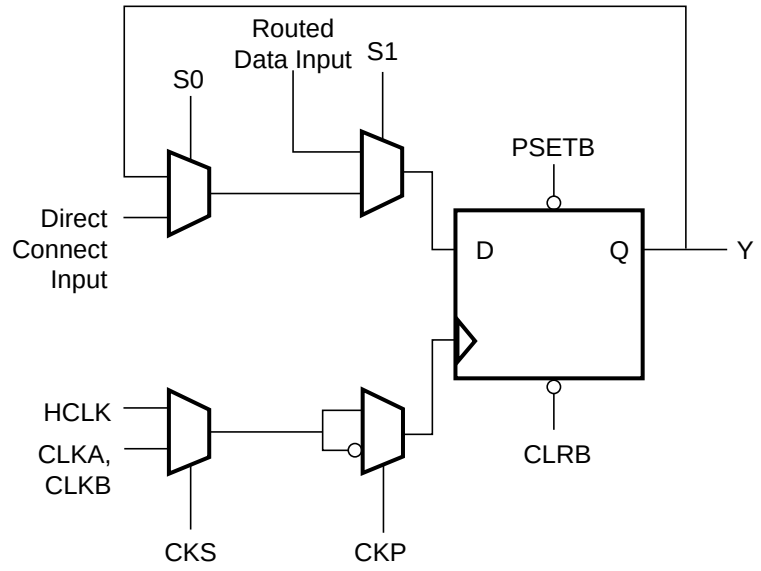


Figure 5 • *R-Cell*

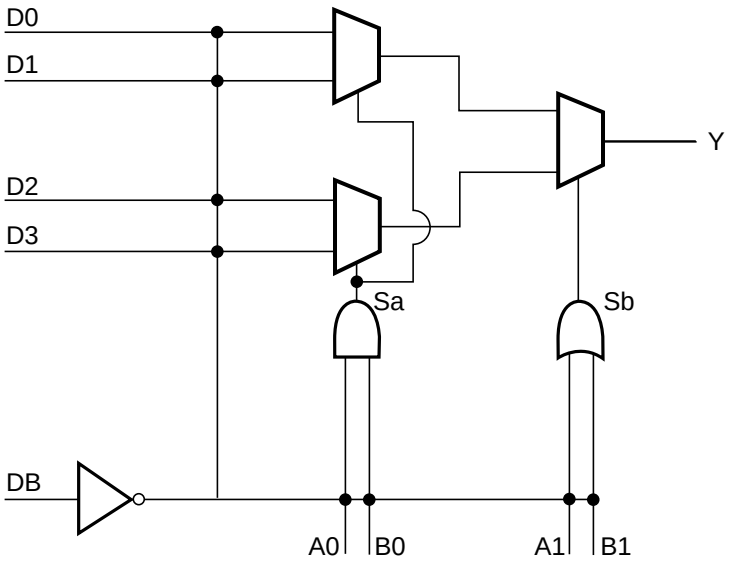


Figure 6 • *C-Cell*

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (see Figure 7). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature significantly more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative new local routing resources called *FastConnect* and *DirectConnect* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (see Figure 8 and Figure 9). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

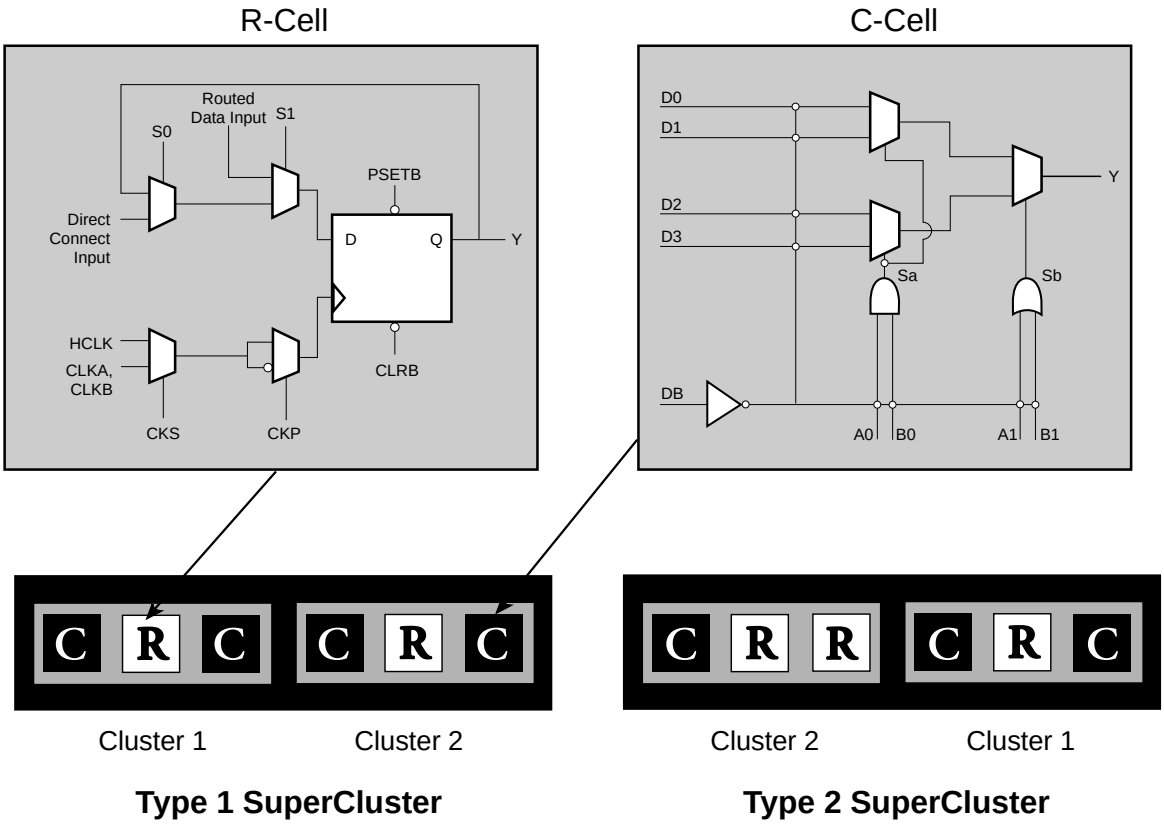


Figure 7 • *Cluster Organization*

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place and route software to minimize signal propagation delays.

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hard-wired from the HCLK buffer to the clock select MUX in each R-cell. This provides a fast propagation path for the clock signal. The hard-wired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal signal logic within the SX device.

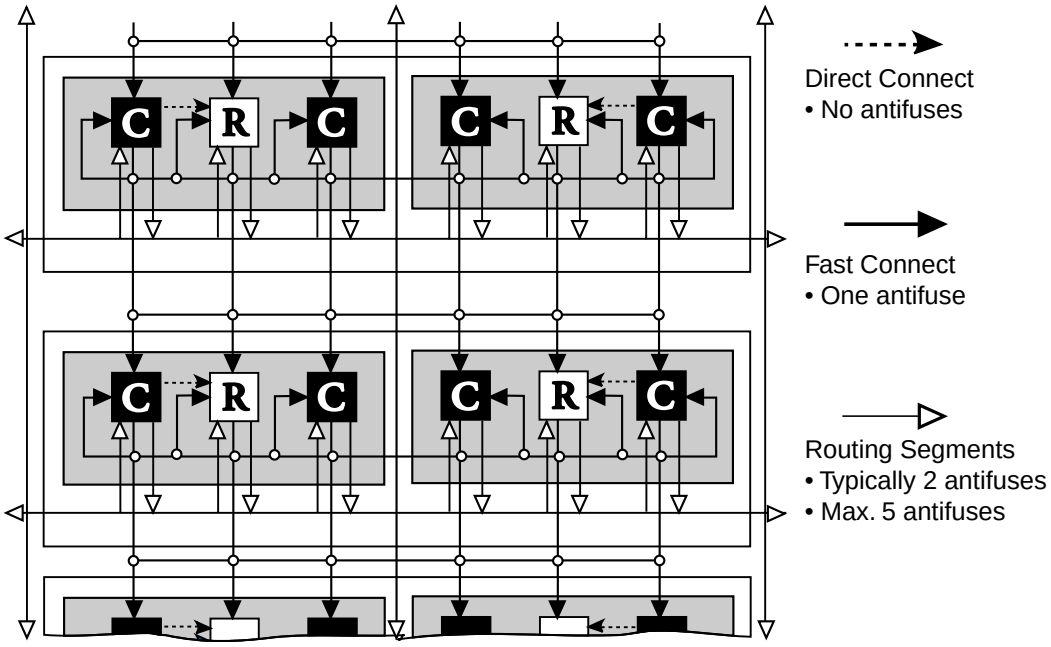


Figure 8 • *DirectConnect and FastConnect for Type 1 SuperClusters*

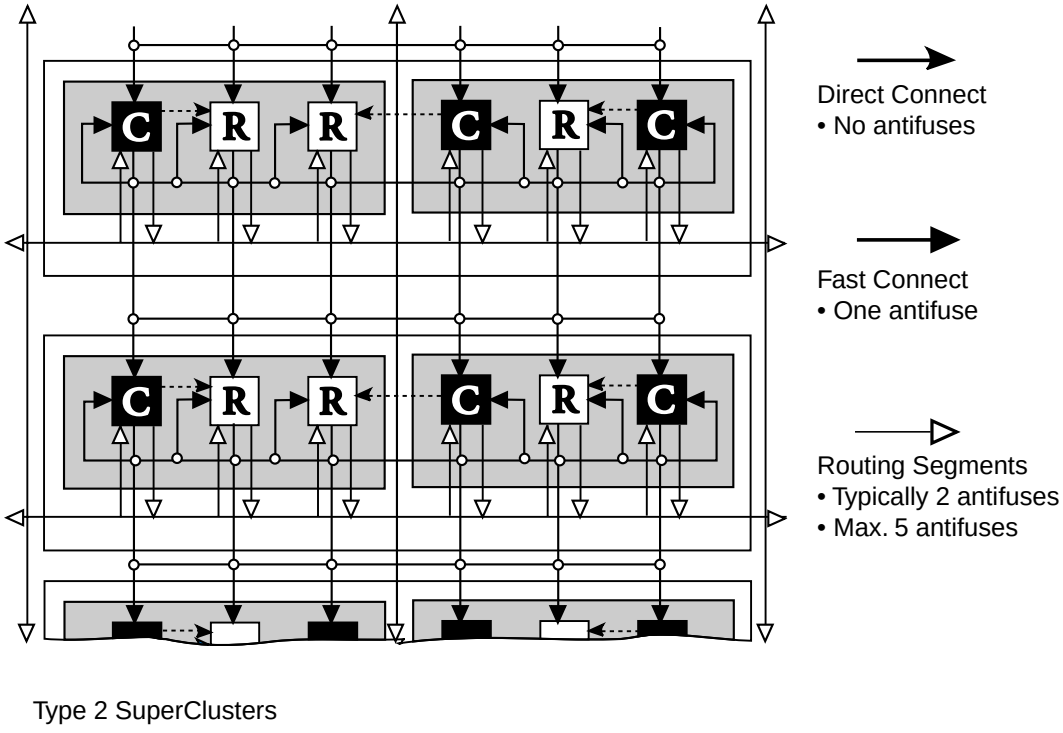


Figure 9 • DirectConnect and FastConnect for Type 2 SuperClusters

3.3V/5V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCR}[3]	DC Supply Voltage[2]	–0.3 to +6.0	V
V_{CCA}[3]	DC Supply Voltage	–0.3 to +4.0	V
V_{CCI}[3]	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	–0.3 to +4.0	V
V_{CCI}[3]	DC Supply Voltage (A54SX16P)	–0.3 to +6.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to +5.0	mA
T_{STG}	Storage Temperature	–40 to +125	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diodes will forward-bias and can draw excessive current.*
3. *V_{CCR} must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.*

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
3.3V Power Supply Tolerance	±10	±10	%V_{CC}
5V Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and military; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
V_{OH}	(I_{OH} = -20uA) (CMOS)	(V_{CC}-0.1)	V_{CC}	(V_{CC}-0.1)	V_{CC}	V
	(I_{OH} = -8mA) (TTL)	2.4	V_{CC}			
	(I_{OH} = -6mA) (TTL)			2.4	V_{CC}	
V_{OL}	(I_{OL}= 20uA) (CMOS)		0.10			V
	(I_{OL} = 12mA) (TTL)		0.50			
	(I_{OL} = 8mA) (TTL)				0.50	
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		20	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Power Dissipation" on page 15.				mA

Power-Up Sequencing

RT54SX16, A54SX16, RT54SX32, A54SX32

V_{CCA}	V_{CCR}	V_{CCI}	Power-Up Sequence	Comments
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Power-Down Sequencing

RT54SX16, A54SX16, RT54SX32, A54SX32

V_{CCA}	V_{CCR}	V_{CCI}	Power-Down Sequence	Comments
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for an RT54SX16 in a CQFP 256-pin package at military temperature and still air is as follows:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{jA}\ (\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{23\text{°C/W}} = 1.09\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	Units
RT54SX16				
Ceramic Quad Flatpack (CQFP)	208	7.5	29	°C/W
Ceramic Quad Flatpack (CQFP)	256	4.6	23	°C/W
RT54SX32				
Ceramic Quad Flatpack (CQFP)	208	6.9	35	°C/W
Ceramic Quad Flatpack (CQFP)	256	3.5	20	°C/W
RT54SX16				
Ceramic Quad Flatpack (CQFP)	208	7.9	30	°C/W
Ceramic Quad Flatpack (CQFP)	256	5.6	25	°C/W
RT54SX16				
Ceramic Quad Flatpack (CQFP)	208	7.6	30	°C/W
Ceramic Quad Flatpack (CQFP)	256	4.8	24	°C/W

Power Dissipation

$$P = [I_{CC}standby + I_{CC}active] * V_{CCA} + I_{OL} * V_{OL} * N + I_{OH} *(V_{CCA} – V_{OH}) * M$$

Where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

The power due to standby current is typically a small component of the overall power. Standby power is shown below for military, worst case conditions (70°C).

I_{CC}	V_{CC}	Power
20mA	3.6V	72mW

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totempole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 1.

$$\text{Power (uW)} = C_{EQ} * V_{CCA}^2 * F \quad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CCA} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CCA}. Equivalent capacitance is frequency-independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values (pF)

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CCA}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_CLK}] \quad (2)$$

Table 2 •

		RT54SX16	A54SX16	RT54SX32	A54SX32
Equivalent Capacitance (pf)					
Modules	C_{EQM}	7.0	3.9	7.0	3.9
Input Buffers	C_{EQI}	2.0	1.0	2.0	1.0
Output Buffers	C_{EQO}	10.0	5.0	10.0	5.0
Routed Array Clock Buffer Loads	C_{EQCR}	0.4	0.2	0.6	0.3
Dedicated Clock Buffer Loads	C_{EQCD}	0.25	0.15	0.34	0.23
Fixed Capacitance (pF)					
routed_Clk1	r_1	120	60	210	107
routed_Clk2	r_2	120	60	210	107
Fixed Clock Loads					
Clock Loads on Dedicated Array Clock	s_1	528	528	1,080	1,080

Where:

m	=	Number of logic modules switching at f_m
n	=	Number of input buffers switching at f_n
p	=	Number of output buffers switching at f_p
q_1	=	Number of clock loads on the first routed array clock
q_2	=	Number of clock loads on the second routed array clock
r_1	=	Fixed capacitance due to first routed array clock
r_2	=	Fixed capacitance due to second routed array clock
s_1	=	Fixed number of clock loads on the dedicated array clock=(528 for A54SX16)
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_{EQCD}	=	Equivalent capacitance of dedicated array clock in pF
C_L	=	Output lead capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz
f_{q2}	=	Average second routed array clock rate in MHz

Determining Average Switching Frequency

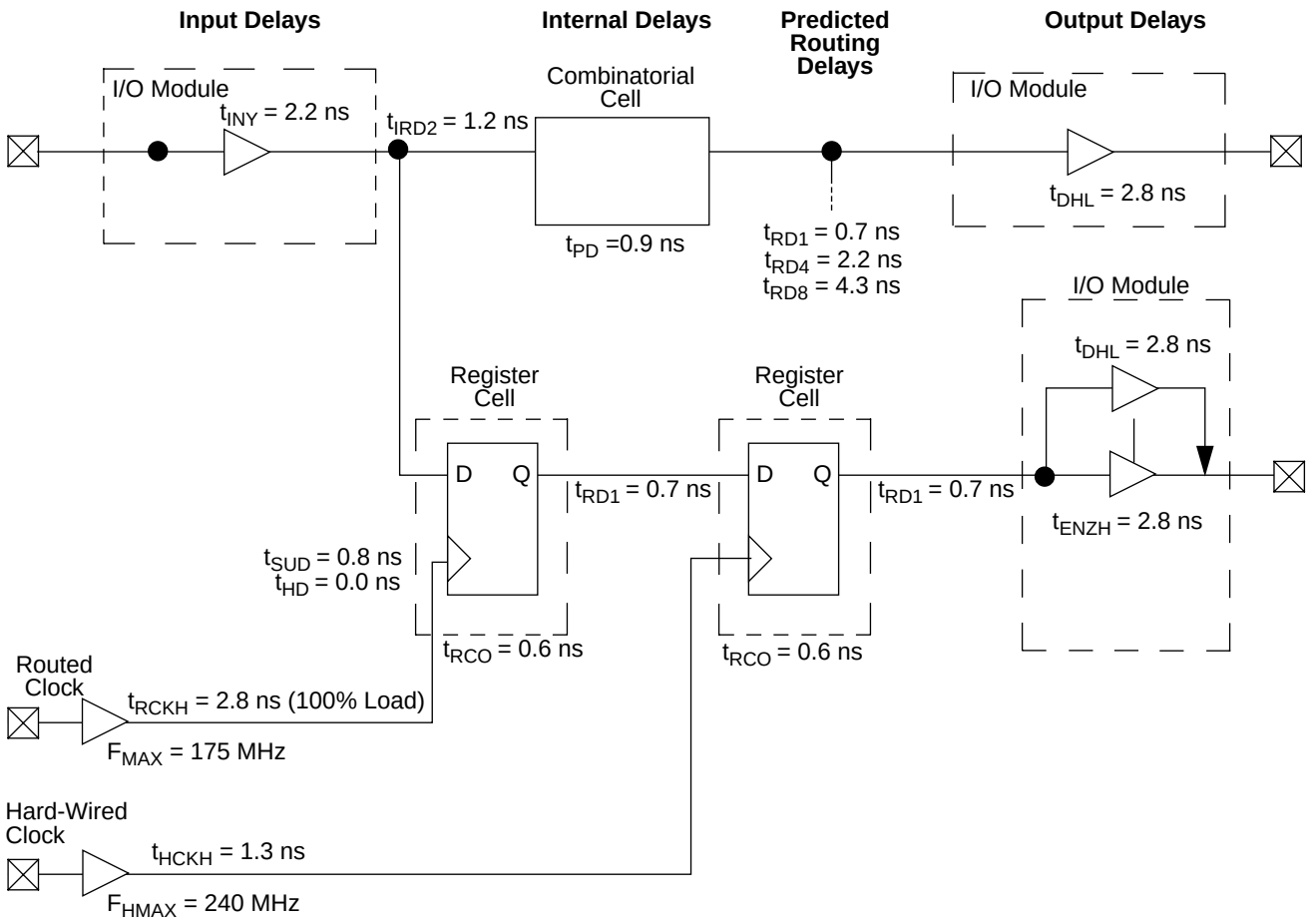
To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Logic Modules (m)	=	80% of modules
Inputs Switching (n)	=	# inputs/4
Outputs Switching (p)	=	# output/4
First Routed Array Clock Loads (q_1)	=	40% of sequential modules
Second Routed Array Clock Loads (q_2)	=	40% of sequential modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F/2
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	F

Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 3.0V)

V_{CCA}	Junction Temperature (T_J)					
	–40	0	25	70	85	125
3.0	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.69	0.77	0.78	0.87	0.92	1.02

54SX Timing Model*



**Values shown for A54SX16-1, worst-case commercial conditions.*

Hard-Wired Clock

External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$
= 2.2 + 0.7 + 0.8 – 1.7 = 2.0 ns

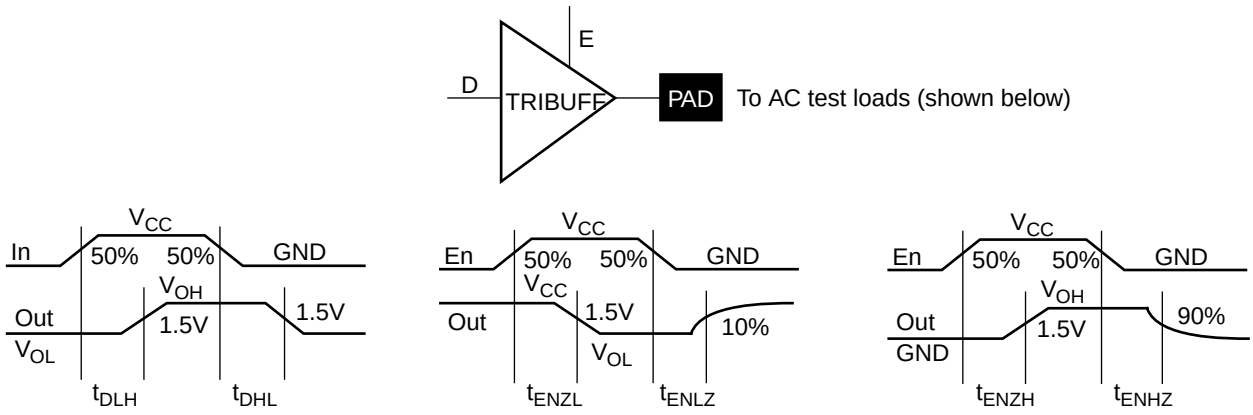
Clock-to-Out (Pin-to-Pin)
= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.7 + 0.6 + 0.7 + 2.8 = 5.8 ns

Routed Clock

External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$
= 2.2 + 0.7 + 0.8 – 2.4 = 1.3 ns

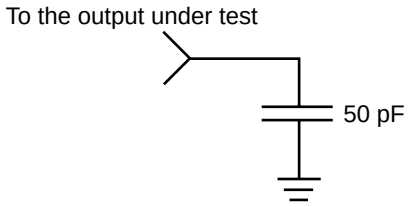
Clock-to-Out (Pin-to-Pin)
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 2.4 + 0.6 + 0.7 + 2.8 = 6.5 ns

Output Buffer Delays

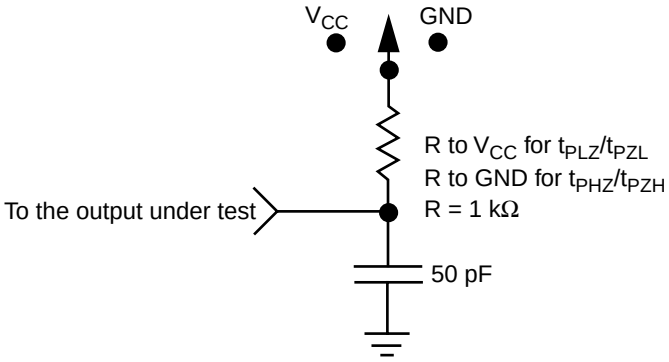


AC Test Loads

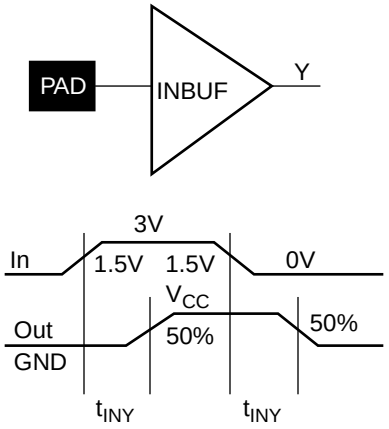
Load 1
(Used to measure propagation delay)



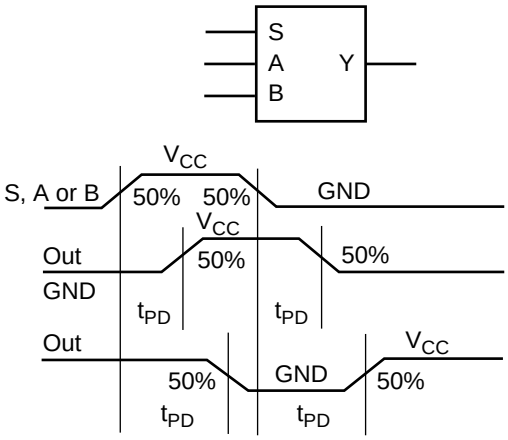
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

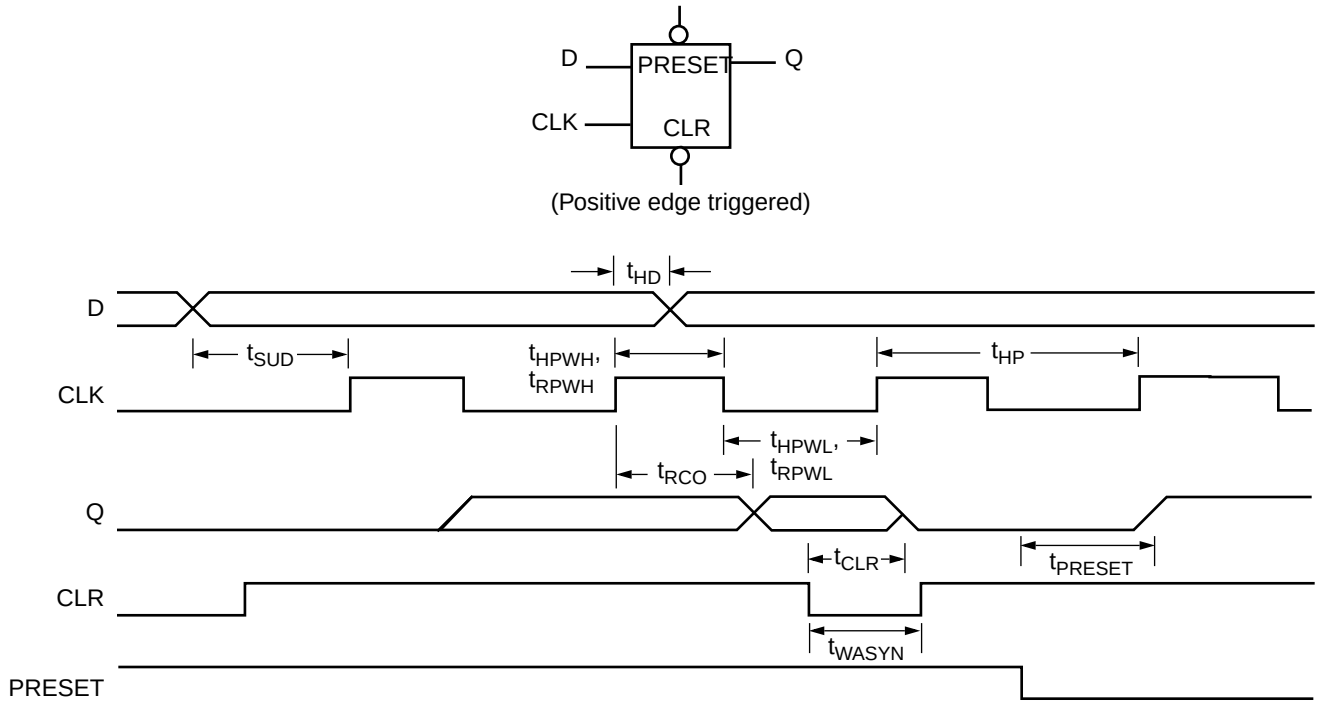


C-Cell Delays



Register Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for 54SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all 54SX family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO=24) routing delays in the data sheet specifications section.

Timing Derating

54SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX16 Timing Characteristics

(Worst-Case Military Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 125°C)

C-Cell Propagation Delays[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		0.9		1.0	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.6		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.7		0.8	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4	ns
t_{RD3}	FO=3 Routing Delay		1.7		2.0	ns
t_{RD4}	FO=4 Routing Delay		2.2		2.6	ns
t_{RD8}	FO=8 Routing Delay		4.3		5.0	ns
t_{RD12}	FO=12 Routing Delay		5.6		6.6	ns
t_{RD18}	FO=18 Routing Delay		9.4		11.0	ns
t_{RD24}	FO=24 Routing Delay		12.4		14.6	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		0.6		0.8	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.8		0.9		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		2.9		ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad-to-Y HIGH		2.2		2.6	ns
t_{INYL}	Input Data Pad-to-Y LOW		2.2		2.6	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		0.7		0.8	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4	ns
t_{IRD3}	FO=3 Routing Delay		1.7		2.0	ns
t_{IRD4}	FO=4 Routing Delay		2.2		2.6	ns
t_{IRD8}	FO=8 Routing Delay		4.3		5.0	ns
t_{IRD12}	FO=12 Routing Delay		5.6		6.6	ns
t_{IRD18}	FO=18 Routing Delay		9.4		11.0	ns
t_{IRD24}	FO=24 Routing Delay		12.4		14.6	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Charateristics(continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.8		3.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.3		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		3.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.5		5.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.2		2.6	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.06	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.08	ns/pF

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

A54SX16 Timing Characteristics (continued)

(Worst-Case Military Conditions)

Dedicated (Hard-Wired) Array Clock Network		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.9		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.4		0.4	ns
t_{HP}	Minimum Period	4.2		4.9		ns
f_{HMAX}	Maximum Frequency		240		205	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.4		2.9	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.7		3.1	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.9		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.8		3.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.6		0.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.8		0.9	ns

RT54SX16 Timing Characteristics

(Worst-Case Military Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 125°C)

C-Cell Propagation Delays[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		1.7		1.8	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.2		0.2	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		1.1		1.3	ns
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		2.2		2.6	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.6	ns
t_{RD4}	FO=4 Routing Delay		4.0		4.7	ns
t_{RD8}	FO=8 Routing Delay		7.8		9.0	ns
t_{RD12}	FO=12 Routing Delay		10.1		11.9	ns
t_{RD18}	FO=18 Routing Delay		17.0		19.8	ns
t_{RD24}	FO=24 Routing Delay		22.4		26.3	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.5		2.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.5		2.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	2.0		2.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.4		5.3		ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT54SX16 Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad-to-Y HIGH		4.0		4.7	ns
t_{INYL}	Input Data Pad-to-Y LOW		4.0		4.7	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		2.2		2.6	ns
t_{IRD3}	FO=3 Routing Delay		3.1		3.6	ns
t_{IRD4}	FO=4 Routing Delay		4.0		4.7	ns
t_{IRD8}	FO=8 Routing Delay		7.8		9.0	ns
t_{IRD12}	FO=12 Routing Delay		10.1		11.9	ns
t_{IRD18}	FO=18 Routing Delay		17.0		19.8	ns
t_{IRD24}	FO=24 Routing Delay		22.4		26.3	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT54SX16 Timing Charateristics (continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		5.1		6.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.1		6.0	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.2		5.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		5.1		6.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		8.1		9.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.0		4.7	ns
d_{TLH}	Delta LOW to HIGH		0.09		0.11	ns/pF
d_{THL}	Delta HIGH to LOW		0.09		0.15	ns/pF

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

RT54SX16 Timing Characteristics (continued)

(Worst-Case Military Conditions)

Dedicated (Hard-Wired) Array Clock Network		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1		3.6	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.5		4.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.8		4.4		ns
t_{HPWL}	Minimum Pulse Width LOW	3.8		4.4		ns
t_{HCKSW}	Maximum Skew		0.8		0.8	ns
t_{HP}	Minimum Period	7.6		8.9		ns
f_{HMAX}	Maximum Frequency		130		110	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.4		5.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		4.9		5.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		5.3		6.0	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		5.1		6.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RPWH}	Min. Pulse Width HIGH	5.6		6.7		ns
t_{RPWL}	Min. Pulse Width LOW	5.6		6.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.1		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.5		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.5		1.7	ns

A54SX32 Timing Characteristics

(Worst-Case Military Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 125°C)

C-Cell Propagation Delays[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		0.9		1.0	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.6		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.7		0.8	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4	ns
t_{RD3}	FO=3 Routing Delay		1.7		2.0	ns
t_{RD4}	FO=4 Routing Delay		2.2		2.6	ns
t_{RD8}	FO=8 Routing Delay		4.3		5.0	ns
t_{RD12}	FO=12 Routing Delay		5.6		6.6	ns
t_{RD18}	FO=18 Routing Delay		9.4		11.0	ns
t_{RD24}	FO=24 Routing Delay		12.4		14.6	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		0.6		0.8	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.8		0.9		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		2.9		ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX32 Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad-to-Y HIGH		2.2		2.6	ns
t_{INYL}	Input Data Pad-to-Y LOW		2.2		2.6	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		0.7		0.8	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4	ns
t_{IRD3}	FO=3 Routing Delay		1.7		2.0	ns
t_{IRD4}	FO=4 Routing Delay		2.2		2.6	ns
t_{IRD8}	FO=8 Routing Delay		4.3		5.0	ns
t_{IRD12}	FO=12 Routing Delay		5.6		6.6	ns
t_{IRD18}	FO=18 Routing Delay		9.4		11.0	ns
t_{IRD24}	FO=24 Routing Delay		12.4		14.6	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX32 Timing Charateristics (continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.8		3.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.3		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		3.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.5		5.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.2		2.6	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.06	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.08	ns/pF

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

A54SX32 Timing Characteristics (continued)

(Worst-Case Military Conditions)

Dedicated (Hard-Wired) Array Clock Network		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.9		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.4		0.4	ns
t_{HP}	Minimum Period	4.2		4.8		ns
f_{HMAX}	Maximum Frequency		240		205	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.4		2.9	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.7		3.1	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.9		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.8		3.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.6		0.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.8		0.9	ns

RT54SX32 Timing Characteristics

(Worst-Case Military Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 125°C)

C-Cell Propagation Delays[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		1.7		1.8	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.2		0.2	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		1.1		1.3	ns
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		2.2		2.6	ns
t_{RD3}	FO=3 Routing Delay		3.1		3.6	ns
t_{RD4}	FO=4 Routing Delay		4.0		4.7	ns
t_{RD8}	FO=8 Routing Delay		7.8		9.0	ns
t_{RD12}	FO=12 Routing Delay		10.1		11.9	ns
t_{RD18}	FO=18 Routing Delay		17.0		19.8	ns
t_{RD24}	FO=24 Routing Delay		22.4		26.3	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.5		2.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.5		2.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	2.0		2.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.4		5.3		ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT54SX32 Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad-to-Y HIGH		4.0		4.7	ns
t_{INYL}	Input Data Pad-to-Y LOW		4.0		4.7	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		2.2		2.6	ns
t_{IRD3}	FO=3 Routing Delay		3.1		3.6	ns
t_{IRD4}	FO=4 Routing Delay		4.0		4.7	ns
t_{IRD8}	FO=8 Routing Delay		7.8		9.0	ns
t_{IRD12}	FO=12 Routing Delay		10.1		11.9	ns
t_{IRD18}	FO=18 Routing Delay		17.0		19.8	ns
t_{IRD24}	FO=24 Routing Delay		22.4		26.3	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT54SX32 Timing Charateristics (continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		5.1		6.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.1		6.0	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.2		5.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		5.1		6.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		8.1		9.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.0		4.7	ns
d_{TLH}	Delta LOW to HIGH		0.09		0.11	ns/pF
d_{THL}	Delta HIGH to LOW		0.09		0.15	ns/pF

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

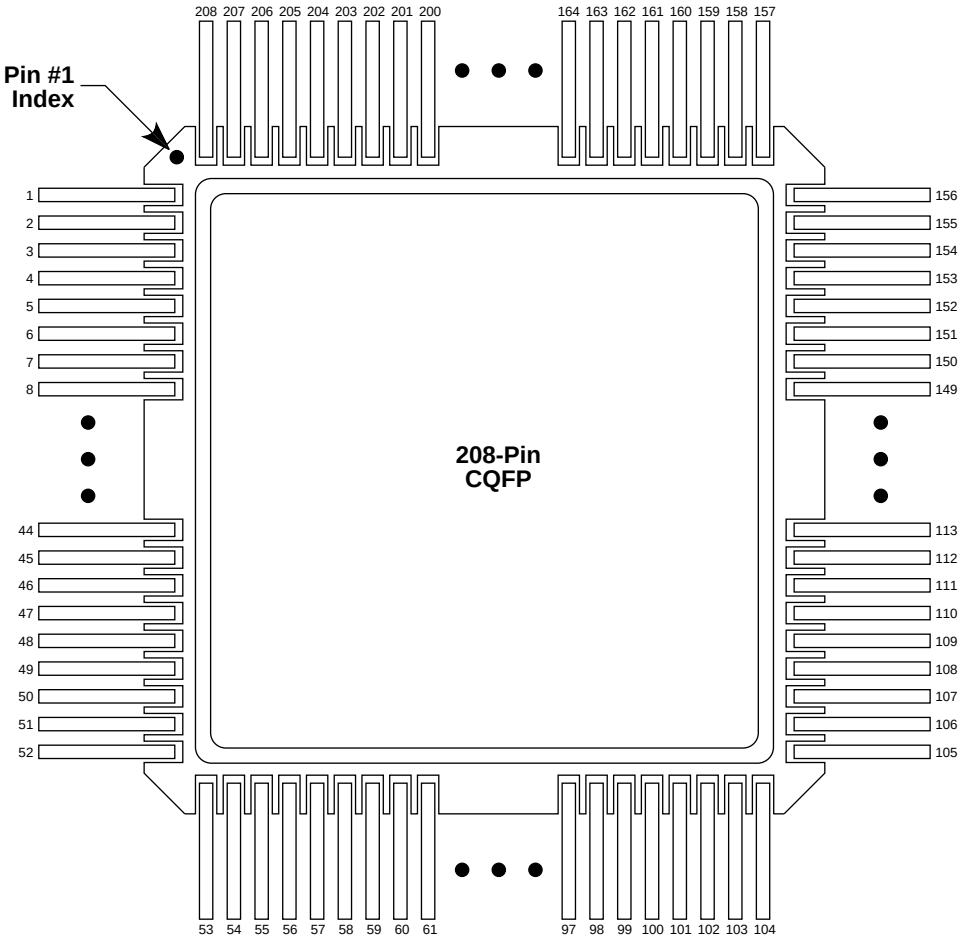
RT54SX32 Timing Characteristics (continued)

(Worst-Case Military Conditions)

Dedicated (Hard-Wired) Array Clock Network		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1		3.6	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.5		4.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.8		4.4		ns
t_{HPWL}	Minimum Pulse Width LOW	3.8		4.4		ns
t_{HCKSW}	Maximum Skew		0.8		0.8	ns
t_{HP}	Minimum Period	7.6		8.9		ns
f_{HMAX}	Maximum Frequency		130		110	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.4		5.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		4.9		5.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		5.3		6.0	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		5.1		6.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RPWH}	Min. Pulse Width HIGH	5.6		6.7		ns
t_{RPWL}	Min. Pulse Width LOW	5.6		6.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.1		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.5		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.5		1.7	ns

Package Pin Assignments

208-Pin CQFP (Top View)



Notes:

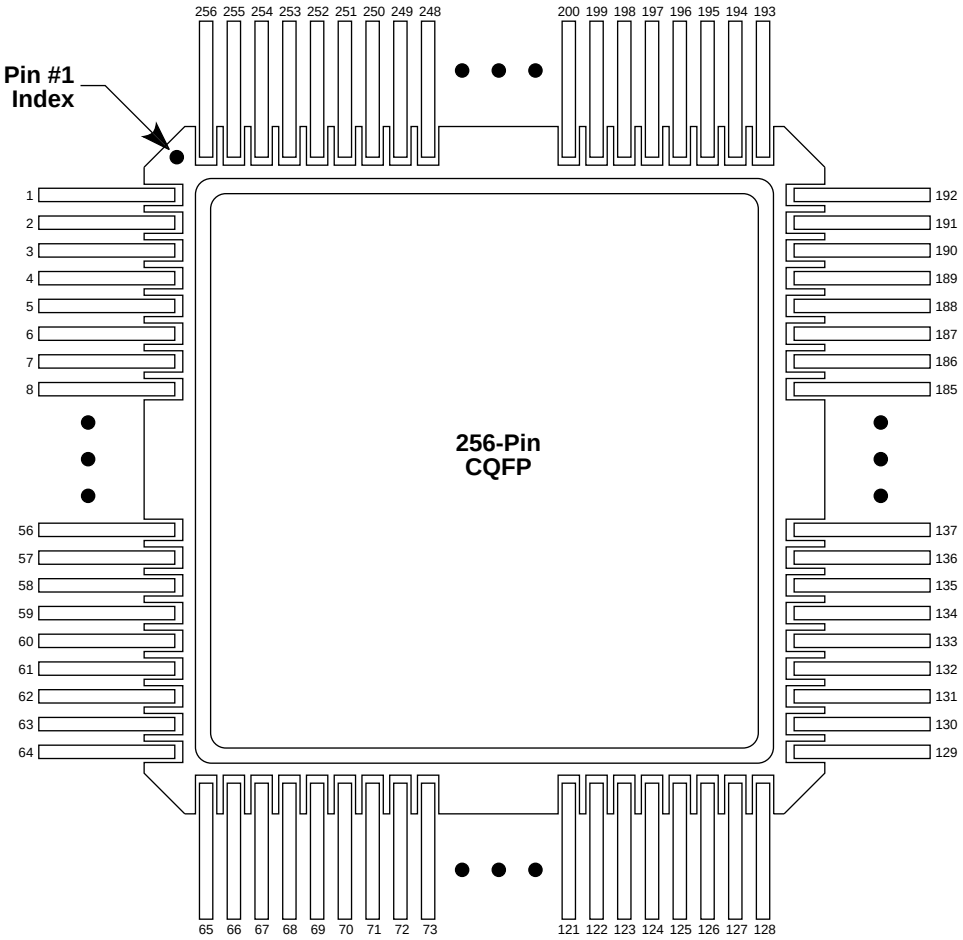
1. *All unlisted pin numbers are user I/Os.*
2. *NC: Denotes No Connection*
3. *MODE should be terminated to GND through a 10K reistor to enable ActionProve usage, otherwise it can be terminated directly to GND.*

208-PIN CQFP

Pin Number	A54SX16 Function	RT54SX16 Function	A54SX32 Function	RT54SX32 Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
11	TMS	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
25	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
26	GND	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND	GND
30	I/O	TRST	I/O	TRST
40	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
52	GND	GND	GND	GND
60	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
65	I/O	I/O	NC	NC
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND	GND
80	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
82	HCLK	HCLK	HCLK	HCLK
98	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
105	GND	GND	GND	GND
114	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
129	GND	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND	GND
132	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
145	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND	GND
148	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
157	GND	GND	GND	GND
164	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
183	GND	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
201	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC: Denotes No Connection*
3. *MODE should be terminated to GND through a 10K reistor to enable ActionProve usage, otherwise it can be terminated directly to GND.*

256-Pin CQFP

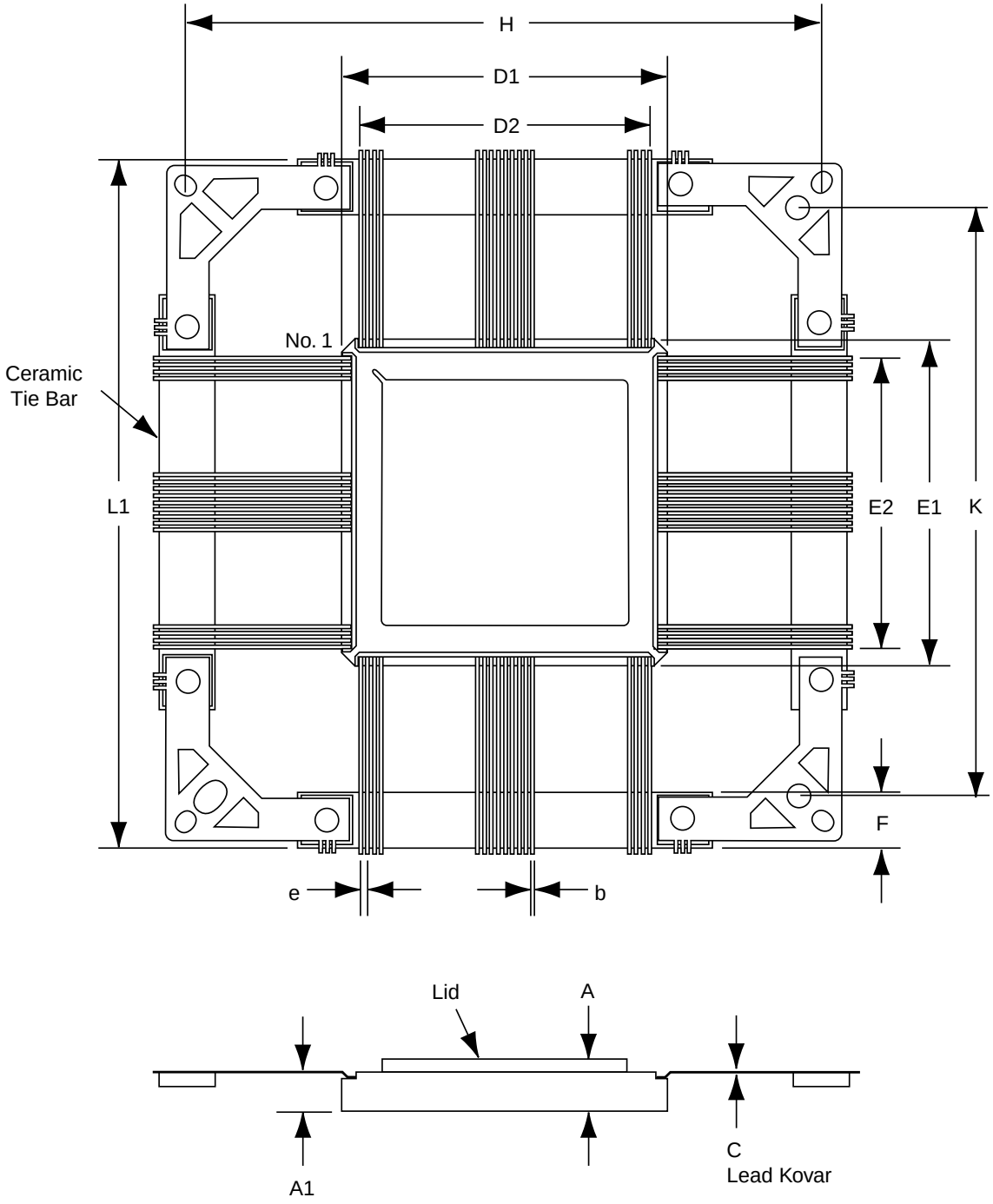
Pin Number	A54SX16 Function	RT54SX16 Function	A54SX32 Function	RT54SX32 Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
11	TMS	TMS	TMS	TMS
12	NC	NC	I/O	I/O
13	NC	NC	I/O	I/O
16	NC	NC	I/O	I/O
20	NC	NC	I/O	I/O
28	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
29	GND	GND	GND	GND
30	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
31	GND	GND	GND	GND
32	NC	NC	I/O	I/O
34	I/O	TRST	I/O	TRST
36	NC	NC	I/O	I/O
41	NC	NC	I/O	I/O
46	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
48	NC	NC	I/O	I/O
51	NC	NC	I/O	I/O
54	NC	NC	I/O	I/O
57	NC	NC	I/O	I/O
59	GND	GND	GND	GND
61	NC	NC	I/O	I/O
63	NC	NC	I/O	I/O
68	NC	NC	I/O	I/O
73	NC	NC	I/O	I/O
77	NC	NC	I/O	I/O
90	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
91	GND	GND	GND	GND
92	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
93	GND	GND	GND	GND
94	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
96	HCLK	HCLK	HCLK	HCLK
98	NC	NC	I/O	I/O
102	NC	NC	I/O	I/O
106	NC	NC	I/O	I/O
110	GND	GND	GND	GND
114	NC	NC	I/O	I/O
118	NC	NC	I/O	I/O
122	NC	NC	I/O	I/O
125	NC	NC	I/O	I/O
126	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
127	NC	NC	I/O	I/O
128	GND	GND	GND	GND
138	NC	NC	I/O	I/O
139	NC	NC	I/O	I/O

256-Pin CQFP (Continued)

Pin Number	A54SX16 Function	RT54SX16 Function	A54SX32 Function	RT54SX32 Function
140	NC	NC	I/O	I/O
141	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
155	NC	NC	I/O	I/O
156	NC	NC	I/O	I/O
157	NC	NC	I/O	I/O
158	GND	GND	GND	GND
159	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
160	GND	GND	GND	GND
161	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
174	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
175	GND	GND	GND	GND
176	GND	GND	GND	GND
178	NC	NC	I/O	I/O
181	NC	NC	I/O	I/O
184	NC	NC	I/O	I/O
187	NC	NC	I/O	I/O
189	GND	GND	GND	GND
191	NC	NC	I/O	I/O
192	NC	NC	I/O	I/O
195	NC	NC	I/O	I/O
200	NC	NC	I/O	I/O
204	NC	NC	I/O	I/O
208	NC	NC	I/O	I/O
219	CLKA	CLKA	CLKA	CLKA
220	CLKB	CLKB	CLKB	CLKB
221	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
222	GND	GND	GND	GND
223	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
224	GND	GND	GND	GND
225	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
227	NC	NC	I/O	I/O
232	NC	NC	I/O	I/O
236	NC	NC	I/O	I/O
239	NC	NC	I/O	I/O
240	GND	GND	GND	GND
243	NC	NC	I/O	I/O
247	NC	NC	I/O	I/O
250	NC	NC	I/O	I/O
253	NC	NC	I/O	I/O
256	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

Package Mechanical Drawings

Ceramic Quad Flatpack (CQFP—Cavity Up)



Notes:

1. *All dimensions are in inches except CQ208 and CQ256 which are in millimeters.*
2. *Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.*
3. *Seal ring and lid are connected to Ground.*
4. *Lead material is Kovar with minimum 60 miconiches gold over nickel.*
5. *Packages are shipped unformed with the ceramic tie bar.*
6. *32200DX – CQ208 has heat sink on the backside.*

Ceramic Quad Flatpack (CQFP)

	CQ208			CQ256		
Symbol	**Min**	**Nom.**	**Max**	**Min**	**Nom.**	**Max**
A	2.78	3.17	3.56	2.28	2.67	3.06
A1	2.43	2.79	3.15	1.93	2.29	2.65
b	0.18	0.20	0.22	0.18	0.20	0.22
c	0.11	0.15	0.17	0.11	0.15	0.18
D1/E1	28.96	29.21	29.46	35.64	36.00	36.36
D2/E2	25.5 BSC			31.5 BSC		
e	0.50 BSC			0.50 BSC		
F	7.05	7.75	8.45	7.05	7.75	8.45
H	70.00 BSC			70.00 BSC		
K	65.90 BSC			65.90 BSC		
L1	74.60	75.00	75.40	74.60	75.00	75.40

Note:

1. *All dimensions are in inches except CQ208 and CQ256, which is in millimeters.*
2. *BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

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