System-on-a-Programmable-Chip Development Board

March 2000, ver. 1.0 User Guide

Features

- Powerful development board for system-on-a-programmable-chip designs
  - Features an APEX™ EP20K400 device
  - Supports microprocessor intellectual property (IP)-based design
- Industry-standard interconnects
  - 10/100 Ethernet with full and half duplexing
  - Peripheral component interconnect (PCI) mezzanine connector
  - High- and low-speed universal serial bus (USB) host supporting the ***Universal Serial Bus Specification ,Revision 1.0***
  - IEEE Std. 1394A at 100, 200, and 400 Mbits/second
  - IEEE Std. 1284 parallel interface
  - 2 RS-232 ports (DCE and DTE)
  - 2 PS/2 ports for mouse and keyboard
- Memory subsystem
  - 2 banks of 1-Mbyte cache memory
  - 64-Mbyte SDRAM in a DIMM socket
  - 4-Mbyte FLASH memory
  - 256-Kbyte EPROM
- Multiple clocks for communications systems design
- Multiple debug ports
  - SignalTap™ embedded logic analyzer
  - IEEE Std. 1149.1 Joint Test Action Group (JTAG)
  - Extended JTAG (EJTAG)
- Supports 50 user I/O lines
- Additional features
  - VGA monitor interface
  - 4 user-defined switches and 6 LEDs
  - Liquid crystal display
  - Application LEDs
- Applications
  - Embedded systems prototyping
  - Communications systems design
  - IP development and debugging

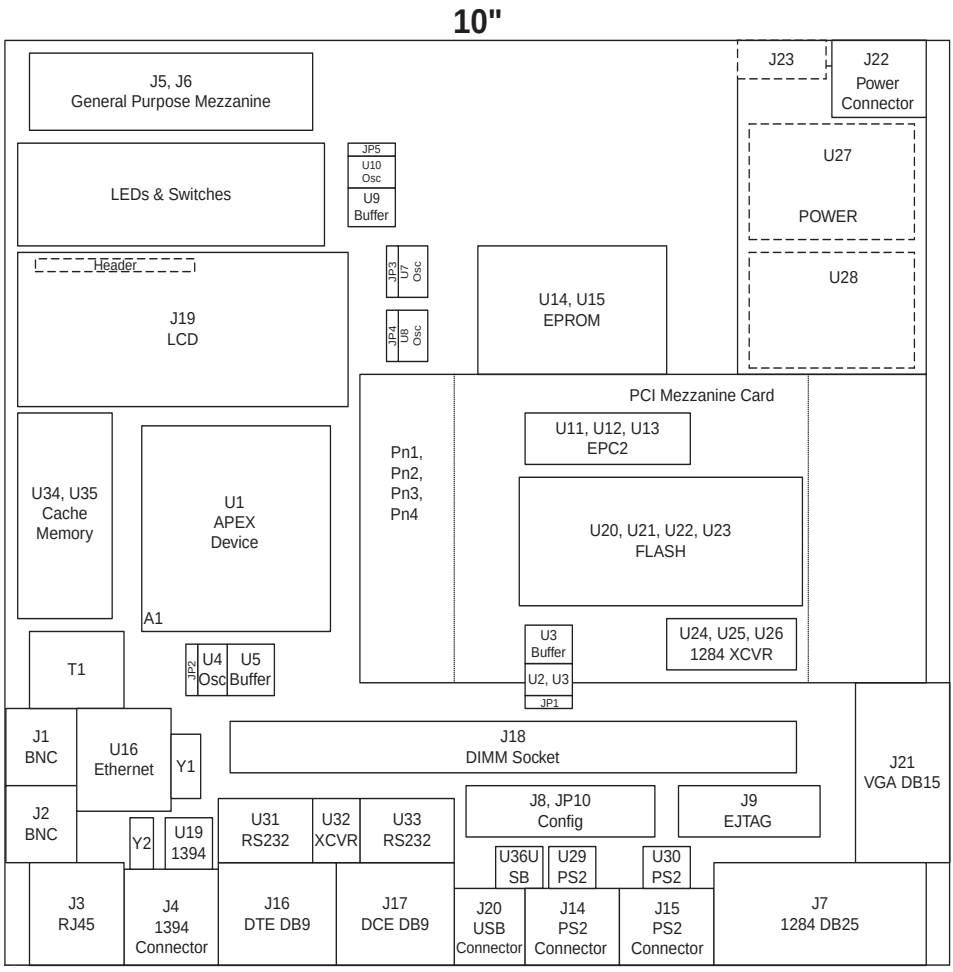
General Description

The Altera® system-on-a-programmable chip board is a development and prototyping platform that provides system designers with an economical solution to hardware verification. Unlike other development boards, the Altera system-on-a-programmable chip board supports a variety of microprocessor-based designs by incorporating memory, debugging, and interface resources.

The board is primarily designed for implementing microprocessor functions and other standard IP functions in the on-board APEX device. The board includes physical interfaces for widely used standard interconnects; control logic for the interconnects can be implemented in the device.

The board also supports EJTAG for development and debugging of MIPS-like microprocessor functions, as well as JTAG for other system testing. For additional analysis, the JTAG port can be used with the SignalTap embedded logic analyzer available with the Altera Quartus™ development software. Figure 1 shows a block diagram of the board.

Figure 1. System-on-a-Programmable-Chip Board Block Diagram



APEX Device

The EP20K400 device (U1 in the block diagram) used on the development board features 423,000 ASIC-equivalent gates in a 652-pin FineLine BGA™ package. The device has 16,640 logic cells and 212,992 RAM bits.

Power

The 8-layer board has four signal layers, a full 3.3-V power plane, and a split 2.5-V, 5.0-V power plane. The APEX device's core power is driven at 2.5 V, and the IEEE Std. 1394 physical layer is driven at 3.3 V. An external 5.0-V power supply is required to power the board. The 3.3-V and 2.5-V supplies are regulated from the 5.0-V supply.

Clocks

The board supports up to six unique clocks that can be selected by the user from a total of ten. The board has two BNC connectors to support communications systems design. The APEX global clock input is driven by a 66-MHz oscillator or driven by an external clock via a BNC connector. The second global clock signal is connected to an oscillator that can drive a PCI function at either 33 or 66 MHz.

Memory

To support processor functions implemented in the APEX device, the board includes a memory system consisting of the following parts:

- Volatile memory: 64 MBytes of synchronous DRAM, organized as 8 Mbytes × 64
- Non-volatile memory: 4 MBytes FLASH memory and a 256-KByte EPROM
- Pipelined cache memory with burst SRAM organized as 256 Kbytes × 32

Interfaces

Table 1 describes the interfaces supported by the board.

Table 1. Development Board Interfaces

Interface	Description
PCI PMC IEEE Std. 1386 connector	This mezzanine connector supports 32 and 64 bits, and 33 and 66 MHz. It is compliant with the ***PCI Local Bus Specification, Revision 2.1***. The designer can use the connector to build an interface to PCI functions in the APEX device.
10/100 Ethernet with full and half duplexing	The Ethernet interface consists of a transceiver and associated discrete devices and allows implementation of an Ethernet media access controller (MAC) in the APEX device.
IEEE Std. 1394A interface	The IEEE Std. 1394A Firewire interface consists of a transceiver/arbiter and associated discrete devices. The physical interface provides a fully IEEE Std. 1394A-compliant cable port at 100, 200, and 400 Mbits per second for a link layer controller (LLC) implemented as a function inside the APEX device.
USB host interface	The USB interface consists of a single host connection with a type A socket. The interface supports both low-speed and high-speed operation without changing the configuration.
User I/O pins	The general-purpose mezzanine interface provides 50 user I/O pins that connect directly to the APEX device, supporting custom interfaces.
IEEE Std. 1284 parallel interface	The parallel interface is a IEEE Std. 1284-compatible transceiver. The transceiver has eight bidirectional data buffers and can be used in extended capabilities port (ECP) mode. The designer can implement the IEEE Std. 1284 control logic in the APEX device.
Debug ports	The board supports in-circuit debugging with the SignalTap embedded logic analyzer, which can be configured in the APEX device, and the MasterBlaster™ cable. The board also has a 50-pin EJTAG header for debugging MIPS-like processors implemented in the APEX device.

General Information

Once power is applied to the board, the LCD display reads "SOPC DEMO BOARD". This program is contained within the EPC2 FLASH PROM devices provided on the board. This message indicates that the EP20K400E device has successfully configured itself, and is functional.

Before the card is handled, anti-static precautions should be taken. The board can be easily damaged without proper anti-static handling.

Initial Setup

To begin using the board, you must complete an initial setup by performing the following steps:

1. Complete the assembly and inspect the board.
2. Apply power.
3. Program the APEX device.
4. Reset the board.

Initial Inspection

To complete the board assembly, you must begin by inserting the SDRAM module (shipped separately) into the DIMM slot. The board should be visually inspected to ensure that it has not been damaged during shipping. Make sure that all components are on the board and that they appear intact. You should then place the board on an anti-static surface.

Applying Power

You can apply power to the board in one of two ways: by using the eight-pin power supply connector (J22), or by using the terminal block (J1) for use with a bench power supply. If you choose to power the board using the terminal block, you must provide a 5.0 V and a ground connection. All of the board components are powered directly from the 5.0-V supply. The 12-V and –12-V inputs are used to provide the required voltages to the PMC mezzanine as required by the specification.

If you apply power through the terminal block (J1), Altera recommends that you use a power supply that is capable of providing 5 A to the 5.0-V input. This value meets the typical maximum requirements for the board. The input current and voltage should be monitored to ensure that adequate power is being provided. You can monitor the current and voltage through the power supply or a digital multimeter.

Depending on testing conditions, the maximum power that may be required by the board is 100 W. This is only required if both mezzanine interfaces are used at the same time, in addition to the devices on the board.

Programming the APEX Device

The APEX 20K device is programmed using the JTAG interface. During initial power up, the APEX 20K device receives configuration data from the EPC2 configuration devices if the devices contain data. If the configuration devices have not been programmed, the APEX device will remain unconfigured.

The APEX device may be programmed directly using the Quartus™ software and the MasterBlaster™ cable.

Refer to Quartus Help for instructions on how to configure devices using the MasterBlaster cable.

After the APEX 20K device has been successfully configured, the green LED D2 will illuminate, indicating that the configuration is complete. At this point, press the Reset switch. If an error occurred during configuration, the red LED D1 will illuminate indicating that the APEX 20K device was not successfully configured. The APEX 20K device must be reprogrammed each time the board is powered down, but will retain its programming information if the board is reset.

The EPC2 configuration device may also be programmed using the MAX+PLUS® II software and a BitBlaster™ download cable. EPC2 configuration devices are accessible using the JTAG interface. The APEX 20K device will only attempt to load configuration data from a EPC2 device on initial power up, which means that if configuration data is changed while the board is turned on, new data will not be loaded into the APEX 20K device until the board is turned off and on.

Initially, EPC2 configuration devices contain a small program that configures the APEX 20K device to display the message "SOPC DEMO BOARD" on the LCD.

Reset

A master reset switch (S1) resets the APEX 20K device through the DEV_CLRn input signal. This is not a board-level reset. Any devices requiring a reset are driven from the APEX device, and the signals will have to be connected to the Reset switch internally. This allows devices on the board to be reset independently from the global reset without requiring additional hardware to prevent contention.

A second switch (S2) is connected to a dedicated low-skew input (pin B17) and is provided as an alternative reset option if the DEV_CLRn input signal is not used. This may be configured internally in the APEX device.

Functional Overview

The following sections give a brief overview of the development board components.

APEX Device

The main component of the system-on-a-programmable-chip development board is the Altera EP20K400E device. The APEX device's package is a 652-pin ball grid array (BGA) package.

For more information about the EP20K400E device, see the *APEX 20K Programmable Logic Device Family Data Sheet*.

Memory Interfaces

Three memory buses interface with the APEX 20K device. The memory buses includes a general-purpose memory bus, a FLASH memory bus, and an EPROM memory bus. The buses provide the development board with four types of memory. Two synchronous SRAM (SSRAM) memory buses are also connected to the APEX device.

DRAM

The SDRAM configuration is compliant with the ***PC SDRAM Unbuffered DIMM Specification, Revision 1.0***. The development board supports configuration types 8 and 9 from this specification. Refer to Table 21 on page 29 for a list of SDRAM control lines.

The address and data lines are shared by all devices connected to the general-purpose memory bus. The SDRAM module does not use all of the address lines, because memory is accessed through both a row and column address.

SDRAM memory is connected to the general-purpose address bus, as defined in the *PC SDRAM Unbuffered DIMM Specification Revision 1.0* for 8M × 64 modules. Module address bits 0 to 11 are connected to the corresponding bits of the general-purpose address bus. Module address bit 12 is unused. Module bank address bits 0 and 1 are connected to general-purpose address bits 13 and 12, respectively.

The SDRAM module is 64-bits wide, while the general-purpose memory data bus is 32-bits wide. To accommodate this, the data bus is doubly loaded, which means that bit 0 of the general-purpose data bus is connected to both bit 0 and bit 32 of the module data bus, and so on.

Improper handling of the Data Byte Mask bits during SDRAM reads can cause contention on the data bus.

The SDRAM byte-enable lines are required to control the data bus. DQM[3..0] accesses the lower 32 bits, and DQM[7..4] accesses the upper 32 bits. Ensure that two byte lanes sharing common bits are not active at the same time. For example, if DQM[0] is enabled, DQM[4] must not be enabled. Refer to Table 19 on page 27 and Table 20 on page 28 for a list of general-purpose data and address lines.

SDRAM is clocked from the same clock source as the APEX device's processor clock for the APEX device to ensure that the interface remains synchronous. This can be either the 66-MHz clock crystal, the variable crystal, or the external input. The SDRAM interface has been tested up to 66 MHz.

FLASH Memory

A 1M × 32 FLASH memory bank is connected to the general-purpose memory bus and provides four Mbytes of memory. The bank is implemented using four 1M × 8 FLASH devices. The device's Micron part number is MT28F800B3WG-10T. Refer to the device data sheet for detailed information on how to access this device. Table 23 on page 30 provides a list of the FLASH control lines.

Because of the significant loading on shared address buses, the FLASH and EPROM memory devices are separated from the other address bus by transceivers. These devices are always enabled so additional control is not required; however, the propagation delay through the transceiver should be taken into account for timing analysis. Table 2 provides information on the devices used to implement the FLASH memory.

Table 2. FLASH Memory Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
U15, U16, U17, U18	MT28F800B3WG-10T	Micron	1M × 32 FLASH Memory
U23, U22, U20	SN74LV245BDW	Texas Instruments	Bus Transceiver

EPROM Memory

The 64K × 32 EPROM memory is implemented using two EPROM devices, each organized as 64K × 16. The bus transceivers used to isolate the EPROM and FLASH devices must be considered for the timing of the EPROM interface. Refer to Table 22 on page 29 for a list of the EPROM control lines. Table 3 lists information on the devices used to implement the EPROM memory. The EPROM memory devices are installed in 44-pin PLCC sockets to allow for easy replacement. The EPROM devices are not configured upon delivery.

Table 3. EPROM Memory Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
U3, U4	NM27LV21OV	Fairchild Semiconductor	64K × 32 EPROM Memory

High-Speed Memory Interface

The board contains two synchronous 256k × 32 SRAM memory banks. Each bank is implemented with one SSRAM device and is separately connected to the APEX device. Both memory devices are synchronous with the processor clock used for the APEX device, and are intended to be used as cache memory for a processor core inside the APEX device.

Table 24, Table 25, and Table 26 on page 31 contains information on the address, data, and control lines for SSRAM bank 1. Tables 27 through 29 lists information on the address, data, and control lines for SSRAM bank 2.

All possible control lines have been connected to the APEX device to allow maximum flexibility of the memory interface. Some control lines may not be required for a particular design and these signals may be left tri-stated, because all control lines are pulled inactive on the board. The parity option for the SSRAM was not connected. Table 4 provides information on the devices used to implement the two SSRAM memory banks.

Table 4. SSRAM Memory Interface Device Reference			
Reference Designator	**Part Number**	**Manufacturer**	**Description**
U21	MT8L256L32DT-10	Micron	256K × 32 SRAM Bank 1
U14	MT58L256L32DT-10	Micron	256K × 32 SRAM Bank 2

Clock Generation & Distribution

The APEX device uses four global clock inputs and one low-skew dedicated input which (used as a clock input) brings the total clock input count to five. Refer to the Jumper Configuration section for detailed information on configuring the clock options on the development board.

The EP20K400E device has four internal phase-locked loop (PLL) circuits, which are available for use on the development board. A jumper is provided to enable the APEX PLL circuitry.

Configuration Interface

The APEX device may be configured using the Quartus software and the MasterBlaster download cable or using the power-up from the three on-board EPC2 configuration devices. Table 18 on page 26 provides a list of configuration signals.

Each time power is applied to the board, the APEX device checks for configuration information stored in the EPC2 configuration devices, and loads any available information. If you change the configuration device's programming information, the board must be turned off and turned on before new information can be loaded into the APEX device.

The EPC2 devices may be programmed through the JTAG interface. Refer to the Jumper Configuration section for detailed information on configuring the JTAG interface. The EPC2 device may not be programmed using the Quartus software and the MasterBlaster download cable. The EPC2 devices are only accessible through the MAX+PLUS II software and the BitBlaster download cable.

If configuration data is targeted at the EPC2 devices, you must first start the Quartus software and select the EPC2 device as an output option to create the required Programmer Object Files (.**pof**) files. If you do not target the EPC2 devices, the Quartus software will generate a single file required to program the APEX device directly.

Serial I/O Interface

The development board contains several serial I/O interfaces. For each serial interface, the transceiver and any associated hardware are provided on the board. The logic controllers must be implemented inside the APEX device. The interfaces on the board include:

- RS-232C (DTE and DCE)
- USB
- IEEE-1394a (Fire Wire)
- PS/2
- 10/100 Base-T Ethernet

RS-232C Interface

There are two RS-232C interfaces provided: Data Terminal Equipment (DTE) and Data Communications Equipment (DCE). All of the hardware lines are provided for each interface. Table 5 provides information on the devices used to implement the RS-232C interface.

Table 5. RS-232C Interface Device Reference

Reference	Part Number	Manufacturer	Description
U32	SP208CT	Sipex	RS-232C DTE transceiver
U34	SP208CT	Sipex	RS-232C DCE transceiver
U33	SN74LV245BDW	Texas Instruments	Bus transceiver

The transceiver used for both interfaces requires a 5.0-V power supply which means the signals going into the APEX device are beyond the maximum 3.3-V input voltage range. A 3.3-volt bus transceiver with 5.0-V tolerant inputs is used to shift signals going into the APEX device. This feature is always enabled so no additional control is required. Since the bus transceiver is always active, the RS-232C input pins cannot be used as outputs or contention will occur. If these pins are not used as part of a design, ensure that they remain in the high-impedence (input) state. See Table 30 on page 33 and Table 31 on page 33 for information on the RS-232C DTE and DCE signals.

USB Interface

The USB interface consists of a single host connection with a type-A socket. The interface is capable of both low- and high-speed operation without changing the configuration. A jumper is provided to allow 5 V to be output to the cable and can be useful when connecting a passive device, such as a mouse, to the port. You should not use this feature if it is not required, because it may cause two power supplies to be connected together. Table 6 provides information on the device used to implement the USB interface.

Table 6. USB Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
U35	SP5301CN	Sipex	USB Transceiver

Table 34 on page 35 provides information on USB control lines.

IEEE-1394a (Firewire) Interface

The IEEE-1394a Firewire interface consists of a transceiver/arbiter and associated components. The physical interface provides a fully IEEE-1394a compliant cable port at 100/200/400 Mbits per second for a Link Layer Controller (LLC) implemented as a core inside the APEX device.

The transceiver/arbiter generates the clock for the LLC inside the APEX device, which is required to synchronize the data coming from the LLC to the transceiver. Eight data lines are provided for data transfers between the LLC and the transceiver. The number of data lines required for the LLC core depends on the transmission rate used for the Firewire bus. The local bus clock always maintains the same frequency. To get the data to the transceiver faster for higher transmission rates, the data bus width must increase. Table 7 shows the data bus requirements for different transmission rates.

Table 7. Firewire Data Bus Usage versus Transmission Rate		
Data Rate (Mbits per Second)	**Data Bus Pins**	**Comments**
100	D[1..0]	Minimum speed for two data pins at 49.152 MHz
200	D[3..0]	Four data pins at 49.152 MHz to double the data rate
400	D[7..0]	All eight data pins used to double the data rate again

The power control pins for the Firewire interface are pulled low, providing a self ID of 0. This means that the interface is not capable of sourcing power to the cable, nor does it require any power from the cable. Table 8 lists information on the device used to implement the Firewire interface.

Table 8. Firewire Interface Device Reference			
Reference Designator	**Part Number**	**Manufacturer**	**Description**
U31	TSB41LV03	Texas Instruments	IEEE-1394a three port transceiver and arbiter

Table 35 on page 35 provides more information on the Firewire control interface signals.

PS/2 Interface

Two PS/2 interfaces are provided with the development board for connecting a mouse and a keyboard. The transceiver provides the correct voltage level translation for the peripheral devices. Power and ground are also provided, because the mouse and keyboard are passive devices. Table 9 provides information on the devices used to implement the PS/2 Interface.

Table 9. PS/2 Interface Device Reference			
Reference	**Part Number**	**Manufacturer**	**Description**
U36	DM7404M	Fairchild Semiconductor	Mouse interface buffer
U37	DM7404M	Fairchild Semiconductor	Keyboard interface buffer

Table 32 on page 34 provides detailed information on the PS/2 keyboard interface, and Table 33 on page 34 provides information on the PS/2 mouse interface.

10/100 Ethernet Interface

The Ethernet interface consists of a transceiver, or PHY, and associated discrete components. This allows you to implement an Ethernet Media Access Controller (MAC) in the APEX device. As shown in Table 36 on page 36, the connections consist of the standard Media Independent Interface (MII) and additional signals. Table 10 provides information on the devices used to implement the Ethernet interface.

Table 10. Ethernet Interface Device Reference

Reference	Part Number	Manufacturer	Description
U29	78Q2120-64CG	TDK	Ethernet MII transceiver

Parallel I/O Interface

The parallel I/O interface consists of an IEEE-1284 compatible transceiver. Table 11 provides information on the device used to implement the parallel port interface.

Table 11. IEEE-1284 Interface Device Reference

Reference	Part Number	Manufacturer	Description
U25	74VHC161284MEA	National Semiconductor	IEEE-1284 (parallel port) transceiver
U24, U26	SN74LV245BDW	Texas Instruments	Bus transceiver

The parallel interface transceiver has eight bidirectional data buffers and can be used in extended capabilities port (ECP) mode. The interface provides enough buffers to connect all ECP control signals from the controller to the peripheral device. There are internal pull-up resistors, eliminating the need for external resistors for the high drive open drain buffers used to drive the data lines connected to the external device.

The parallel port interface uses a 5.0-V supply, which means the output signals are also set to 5.0 V. Two 3.3-V supply bus transceivers with 5.0-V tolerant inputs are used on APEX device input signals. U24 is used for the bi-directional data bus and the transceiver direction is connected to the direction control for the IEEE-1284 transceiver. No additional control is required; however, the timing for the bus transceiver must be considered as part of the interface. The second transceiver is always enabled. If the signals are not used, the APEX device pins must always be left in the high-impedence (Input) state.

For further information on the parallel port control lines, see Table 37 on page 37 and Table 38 on page 39.

For the parallel port interface to operate normally, the APEX device contains the host controller and the external device serves as the peripheral. The parallel port interface may also be configured so that the APEX device acts as a peripheral device. Port direction is controlled by nine jumpers (JP19-34). Jumper positioning determines the direction of the parallel port. When all jumpers are placed in the 1-2 position, the parallel port will be in host mode, which is required for normal operation. By placing all jumpers in the 2-3 position, the control lines directions are reversed and the board interface operates as a peripheral. For proper operation, all jumpers must be in the same position. Table 37 on page 37 and Table 38 on page 39 provides information on the parallel port control lines.

Mezzanine Interfaces

A PCI Mezzanine Card (PMC) site included on the board. This is a 32/64-bit 33/66-MHz capable interface, and is compliant with ***PCI Local Bus Specification, Revision 2.2***.

See the following references for more detailed information on the PMC interface. The interface is 3.3-V compliant.

- ***PCI Local Bus Specification, Revision 2.2***.
- Standard for Physical and Environmental Layers for PCI Mezzanine Cards: PMC IEEE P1386.1.
- Standard for a Common Mezzanine Card Family: CMC IEEE P1386/Draft 2.0.

For detailed information on the PCI interface and connector pinouts, refer to PMC and CMC specifications (IEEE-1386). No user I/O pins are provided for the PMC interface. All user I/O pins from the PMC are provided through connectors mounted directly on the mezzanine card. Clearance is provided on the board to support a PMC with user I/O connectors as required by the CMC specification.

Table 40 on page 41, Table 41 on page 42, and Table 42 on page 42 list the PMC signal pin assignments.

General-Purpose Mezzanine Interface

The general-purpose mezzanine interface provides an additional custom interface prototyping area. The interface includes 38 general-purpose user I/O lines, power (3.3 V, 5 V, 12 V, and –12 V), and clock pins. The clock interface is synchronous with the main processor and memory clock to ease the effort required to interface with the rest of the board.

The general purpose mezzanine interface also includes a JTAG chain so that devices can be programmed using the same interface as devices on the development board.

External feedback pins for the PLL circuitry are connected to the general-purpose mezzanine interface as well. This allows an optional method for externally connecting these signals, if required. They may also be internally connected to the APEX device.

Table 43 on page 43, and Table 44 on page 44 provide a list of the general-purpose mezzanine signal pin assignments.

Display & Switch Interfaces

A two-row 16 character liquid crystal display (LCD) is provided on the board. The LCD has an integrated controller and operates off a single 5.0-V supply. The LCD display is an Emerging Technologies ED162A0RU that uses a Hitachi HD44780U controller. See Table 12.

Table 12. IEEE-1284 Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
J5	ED162A0RU	Emerging Display Technologies	2 × 16 Character Display (connected through a 1 × 16 header)
N/A	HD44780U	Hitachi	LCD controller (installed on the display)
U7	SN74LV245BDW	Texas Instruments	Bus Transceiver

The LCD is powered from a 5.0-V supply, which means the output signal levels are 5.0-V TTL. A 3.3-V bus transceiver is used to translate signal levels to match with the APEX device inputs. The direction of the bus transceiver is controlled by the read/write line of the display, so no additional control logic is required.

Table 46 on page 45 lists the LCD signal pin assignments.

LED Interface

The development board has several LEDs that tie user-defined functions and application-specific functions directly to the APEX device. Table 47 on page 46 provides more information on APEX device pins connected to LEDS.

Six LEDs are connected directly to the APEX device I/O pins. The LEDs illuminate when an I/O pin is driven low. These LEDs consist of:

- Four green LEDs (LED1, LED2, LED3, LED4)
- Two red LEDs (LED5, LED6)

LEDs are also used for specific application functions on the board, such as the configuration and Ethernet interfaces. The green LEDs are also used as PLL lock indicators. Table 13 lists the LEDs and their functions.

Table 13. Application LED Usage

LED Reference	Application	Use
D2	Init_Done	Indicates that the APEX configuration is complete
D1	NStatus	Indicates an Error in the APEX Configuration
D5	LEDL	Ethernet: Link Up (normally on)
D6	LEDTX	Ethernet: TX (On during TX)
D7	LEDRX	Ethernet: RX (On During RX)
D4	LEDCOL	Ethernet: Collision in Half Duplex Mode (Off in Full Duplex Mode)
D8	LEDBTX	Ethernet: 100 BaseT Connection (Off for all other connection interfaces)
D9	LEDBT	Ethernet: 10 BaseT Connection (Off for all other connections)
D10	LEDFX	Ethernet: Full Duplex On (Off in half duplex)

VGA Monitor Interface

The VGA monitor interface is a restricted version of VGA, and is compliant with the monitor interface used with the Altera University Program Design Laboratory Package.

The VGA monitor interface includes three-color outputs that may be turned on or off. High output on any of the R, G, or B outputs results in a 0.7-V nominal signal at the VGA connector pin. Low output results in 0-V output at the VGA connector. The output is achieved with a resistor/diode network between an APEX device I/O pin and the connector. The horizontal and vertical sync signals are connected directly from the APEX device. Table 45 on page 45 provides more information on the VGA interface.

User-Defined Switches

Four momentary switches with integrated LEDs are connected to the APEX device. Pressing the switch causes a low singal to be input to the APEX device pin until the switch is released.

The (S1) switch is the device-wide clear input pin is connected to DEV_CLRn on the APEX device. Another switch (S2) is connected to a low-skew dedicated input and functions as a reset input for applications where DEV_CLRn is not applicable. The remaining switches are connected to I/O pins and can be configured internally as desired. Debouncing is provided for these signals and must be done internally. Table 46 on page 45 provides more information on the switch interface.

Test & Debug Features

The development board includes three test features:

- The SignalTap Embedded Logic Analyzer, which uses a JTAG interface to allow access to activity on internal nodes.
- An EJTAG connector, which can be used for debugging processor cores.
- Test connectors provided for debugging with a logic analyzer.

SignalTap Embedded Logic Analyzer

The development board supports in-circuit debugging with the SignalTap logic analyzer using the Quartus software and MasterBlaster download cable.

EJTAG Interface

A 52-pin header is provided for use with an EJTAG interface for debugging a MIPS processor core in the APEX device. Although the EJTAG interface supports normal JTAG signals, it is not included as part of the programming chain. The EJTAG interface uses normal I/O pins. Before the APEX device is completely configured, these I/O pins are not available for general use, which means that the external JTAG chain could be broken.

Refer to the MIPS EJTAG Debug Solution Rev 2.0 for a detailed reference on using the EJTAG interface.

Table 39 on page 40 lists the APEX device pins used for the EJTAG interface.

Test Connectors

Six test connectors are provided on the development board. These allow external monitoring of the high-speed memory interfaces. Refer to Table 58 on page 52, through Table 63 on page 55 for pin definitions of all of the test connectors.

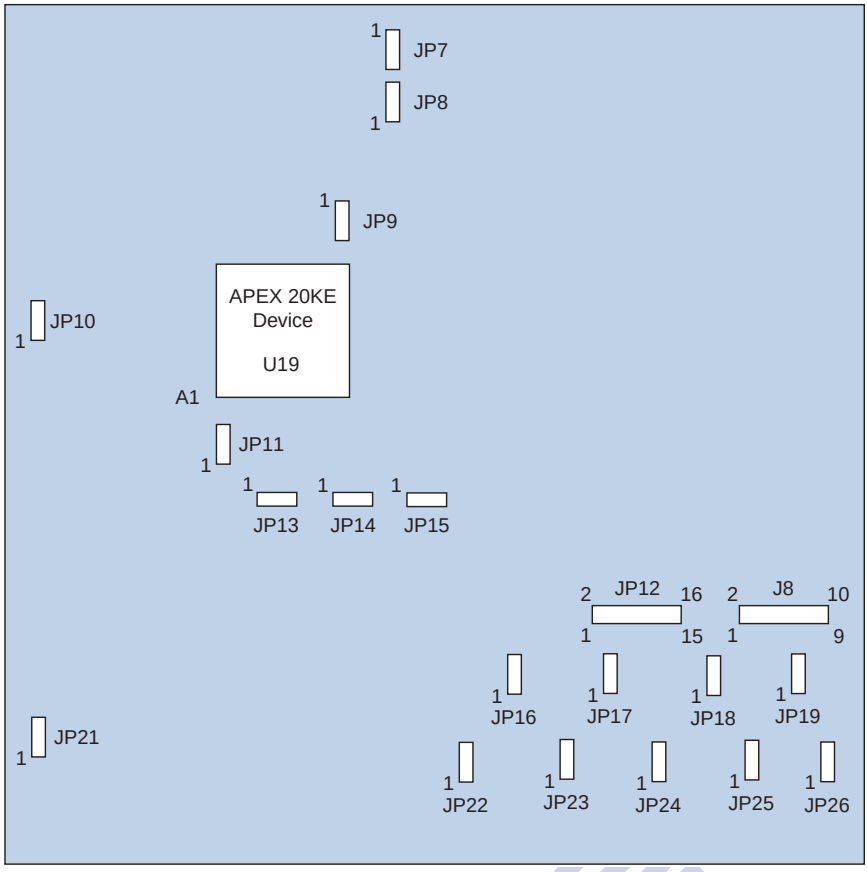
Jumper Configuration

The jumpers on the SOPC serve several functions:

- Clock distribution
- Enabling the PLL interface
- JTAG configuration
- Optional USB power setting
- IEEE 1284 parallel interface configuration

Figure 2 illustrates the development board jumper configuration.

Figure 2. Development Board Jumper Locations



Clock Distribution

Five inputs on the APEX device are used for clocks. Four are global clock inputs, and one is a low-skew dedicated input. Jumpers JP9 - JP14 are used to select different clock inputs. Table 14 lists all clock sources on the development board. Table 15 lists the APEX device pins used as clock inputs, and the possible sources of the clock inputs for each pin. Table 16 and Figure 3 illustrate how to configure the clock selection jumpers.

Table 14. SOPC Clock Sources

Source Number	Name	Source Pin	Description
1	Memory/Processor Clock	U28	This is the 66 MHz main clock provided to all the synchronous memory and a processor core
2	PMC Clock (33MHz)	U27	33 MHz Oscillator for a 33-MHz PCI core and PMC card
3	PMC Clock (66 MHz)	U6	66 MHz Oscillator for a 66 MHz-PCI core and PMC card
4	Ethernet TX Clock	U29 pin 27	TX Clock output from Phy
5	Ethernet RX Clock	U29 pin 24	RX Clock output from Phy
6	External Source	J6	External source for the Memory/Processor clock
7	VGA Clock	U2	25.175 Oscillator for VGA interface
8	USB Clock	U8	48 MHz Oscillator for USB interface
9	Firewire Clock	U31 pin 2	Firewire SYSCLCK output from transceiver
10	EJTAG TCK	J10 Pin 9	TCK input from EJTAG Header
11	Variable Oscillator	U30	Socket provided for populating various clock frequencies

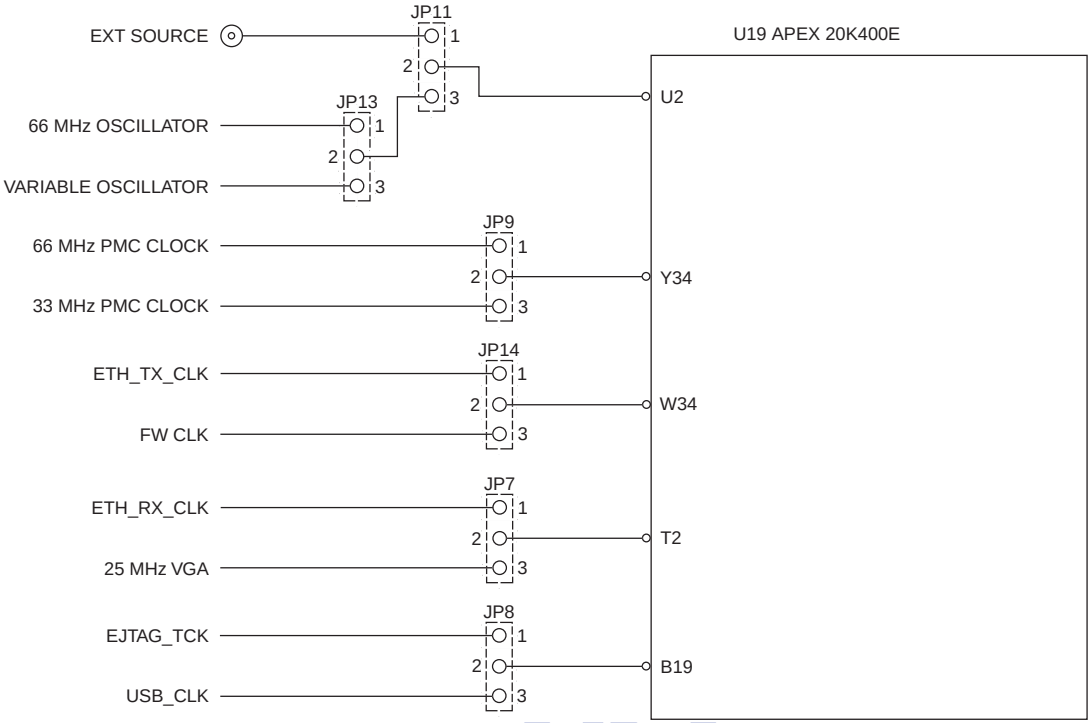
Table 15. EP20K400E Clock Input Pins and Sources

Pin	Description	Clock Inputs to Pin
U2	Global Clock Input	Clock Source 1, 6, and 11
Y34	Global Clock Input	Clock Source 2, and 3
W34	Global Clock Input	Clock Source 4, and 9
T2	Global Clock Input	Clock Source 5, and 7
B19	Low Skew Input	Clock Source 8, and 10

Table 16. Clock Jumper Configuration

Clock Description	Header Designation	Jumper Position and Input Selected	
		1-2	2-3
PMC Clock	JP9	66 MHz	33 MHz
Memory Clock	JP11	External Source J6	Output of JP13
VGA/Ethernet RX Clock	JP7	VGA 25.175 MHz	Ethernet RX
EJTAG/USB Clock	JP8	EJTAG	USB 48 MHz
Mezzanine Clock	JP13	66 MHz	Variable Oscillator
Firewire/Ethernet TX Clock	JP14	Ethernet TX	Firewire Clock

Figure 3. Clock Source Jumper Configuration



Jumpers JP11 and JP13 are used to select the one clock input. JP11 selects between the 66 MHz or the socketed variable oscillator. JP13 selects between the output from JP11 and the external clock input.

The master clock input to the development board is the 66-MHz oscillator. This clock is used for all synchronous memory interfaces as well as the general-purpose mezzanine interface and the APEX device.

During development, it may be necessary to run the interface at a slower clock rate. To accomplish this you may use either the external clock input or the variable oscillator.

The external oscillator is a BNC cable input (J6) that can be used to input a signal from a laboratory signal generator. The variable oscillator is a four-pin socket that supports a variety of 5.0-V oscillators.

The development board operates best for synchronous memory interface frequencies up to 66 MHz. You may attempt higher frequencies without risk of damaging the board, but results may be unpredictable.

JTAG Configuration

All devices that can be programmed through the JTAG interface are connected to a 2 × 8 0.1 inch configuration header, JP12. The devices connected to the chain (in order) are:

- EP20K400E
- EPC2 Configuration Devices
- PMC Interface
- General-Purpose Mezzanine Interface

Table 17. JTAG Chain Configuration

Device	Bypass Jumper Setting (Pins for JP12)	Chained Jumper Settings (Pins for JP12)
APEX 20KE Device	1-3	1-2 3-4
EPC2 Configuration Device	5-7	5-6 7-8
PMC Interface	9-11	9-10 11-12
General-Purpose Mezzanine Interface	13-15	13-14 15-16

If a device is not included in the programming chain, it must be bypassed at JP12 or else the JTAG chain will be broken. For example, if the APEX device is programmed alone, shunts would be installed as follows:

- JP12 pins 1-2
- JP12 pins 3-4
- JP12 pins 5-7
- JP12 pins 9-11
- JP12 pins 13-15

IEEE 1284 Parallel Interface

The IEEE 1284 parallel interface can be configured so that the development board can operate as a host or as a peripheral. To configure the interface to use the board as a host, jumpers JP19 to 34 must be set to the 1-2 position. To configure the interface to use the SOPC board as a peripheral, jumpers JP19 to 34 must be set to the 2-3 position.

The same female connector is used when configuring the interface for host and peripheral mode. When the interface is in peripheral mode, it does not meet the standard mechanical requirements, but it meets the standard electrical requirements. A 25-pin gender adapter is required to allow a normal peripheral cable be used with the development board.

APEX Pin Assignments

The main component of the development board is the EP20K400E device. The pins on the APEX device are assigned to functions on the board. When generating intellectual property (IP) cores for the APEX device, the pins must be used as defined to avoid damaging the device. The following sections list the interfaces and dedicated pins on the board. Any pins that are not used for a design should be left in the high-impedence (input) state to avoid accidentally causing contention.

Configuration

The APEX device pins listed in Table 18 are used exclusively for configuring the device. Refer to the Getting Started section for more information about configuring the APEX device.

Table 18. EP20K400E Configuration Pins

Signal Name	APEX Pin	Description
MSEL0	U35	Configuration Mode select (tied to GND)
MSEL1	W35	Configuration Mode select (tied to GND)
NSTATUS	AN17	OE for EPC2s
NCONFIG	W32	INIT for EPC2s
DCLK	U3	Data Clock For EPC2s
CONF_DONE	AM17	CS for EPC2s
nCE	U1	Not Connected
DATA0	U4	Serial input for EPC2 Configuration Data
TDI	W1	JTAG Data In
TDO	C17	JTAG Data Out (to next device in the chain)
TCK	AN19	JTAG Clock
TMS	AM19	JTAG Mode Select
TRST	D19	JTAG Reset (Pulled High)
DEV_CLRn	T6	Global Reset for the device

General-Purpose Memory Interface

The general-purpose memory bus has a shared addresses and data with the SDRAM, FLASH, and configuration devices. Separate control lines are used for each type of memory.

General-Purpose Memory Data Bus

The SDRAM module is 64-bits wide, and the general-purpose memory data bus is 32-bits wide. To allow access to the entire SDRAM memory array, data bus pins are doubled. This means that the upper half of the data bus is connected to the lower half. For example, GPM_D(0) is connected to data pin 0 and data pin 32 on the SDRAM DIMM. Ensure that only 32 bits of the SDRAM data bus are enabled at a time (D[31..0] or D[63..32]) to avoid contention.

Table 19. General-Purpose Memory Data Bus Pin Assignment

Signal Name	APEX Pin	Signal Name	Apex Pin
GPM_D(0)	AP16	GPM_D(16)	AR10
GPM_D(1)	AP20	GPM_D(17)	AR11
GPM_D(2)	AP21	GPM_D(18)	AR12
GPM_D(3)	AP22	GPM_D(19)	AR13
GPM_D(4)	AP23	GPM_D(20)	AR14
GPM_D(5)	AP24	GPM_D(21)	AR15
GPM_D(6)	AP25	GPM_D(22)	AR16
GPM_D(7)	AP26	GPM_D(23)	AR20
GPM_D(8)	AR2	GPM_D(24)	AR21
GPM_D(9)	AR3	GPM_D(25)	AR22
GPM_D(10)	AR4	GPM_D(26)	AR23
GPM_D(11)	AR5	GPM_D(27)	AR24
GPM_D(12)	AR6	GPM_D(28)	AR25
GPM_D(13)	AR7	GPM_D(29)	AR26
GPM_D(14)	AR8	GPM_D(30)	AR27
GPM_D(15)	AR9	GPM_D(31)	AR28

General-Purpose Memory Address Bus

The general-purpose memory address bus is also shared, but all 20 pins are not required for each memory device. The address lines on the FLASH and configuration device are isolated from the SDRAM by bus transceivers. These devices are always enabled, so additional control is not required, but the delay on the address lines need to be included for timing analysis. The SA[2..0] lines on the SDRAM module are used as the serial configuration address lines, so the exact module configuration may be read by the memory controller.

Table 20. General Purpose Memory Address Bus Pin Assignment

Signal Name	APEX Pin	Connected to		
		DRAM / Name	FLASH	EPROM
GPM_A(0)	AN16	A0	DQ15/A-1	A0
GPM_A(1)	AN20	A1	A0	A1
GPM_A(2)	AN21	A2	A1	A2
GPM_A(3)	AN22	A3	A2	A3
GPM_A(4)	AN23	A4	A3	A4
GPM_A(5)	AN24	A5	A4	A5
GPM_A(6)	AN25	A6	A5	A6
GPM_A(7)	AP3	A7	A6	A7
GPM_A(8)	AP4	A8	A7	A8
GPM_A(9)	AP5	A9	A8	A9
GPM_A(10)	AP6	A10	A9	A10
GPM_A(11)	AP7	A11	A10	A11
GPM_A(12)	AP8	BA1	A11	A12
GPM_A(13)	AP9	BA0	A12	A14
GPM_A(14)	AP10	NC	A13	A14
GPM_A(15)	AP11	NC	A14	A15
GPM_A(16)	AP12	NC	A15	NC
GPM_A(17)	AP13	SA0	A16	NC
GPM_A(18)	AP14	SA1	A17	NC
GPM_A(19)	AP15	SA2	A18	NC

SDRAM Control Lines

The SDRAM_DQM[7..0] lines are used to enable the SDRAM outputs. Because the data bus pins are doubled-up on the SDRAM DIMM, you may not enable both halves of the data bus at the same time. For example, if SDRAM_DQM[0] is enabled, SDRAM_DQM[4] cannot be enabled or contention will occur. Tables 21 through 30 show the pin-outs.

Table 21. SDRAM Control Signal Pin Assignment

Signal Name	APEX Pin	Description
SDRAM_RAS	AD1	Row Address Strobe
SDRAM_CAS	AD2	Column Address Strobe
SDRAM_WE#	AC1	Write Enable
SDRAM_CS1	AC2	Chip Select
SDRAM_CS2	AF5	Chip Select
SDRAM_CKE	AC4	Clock Enable
SDRAM_SDA	AC5	Serial EPROM Data output
SDRAM_SCL	N31	Serial EPROM Clock input
SDRAM_DQM(0)	AA1	Data Bus Enable (D0-7)
SDRAM_DQM(1)	AA2	Data Bus Enable (D8-15)
SDRAM_DQM(2)	AA3	Data Bus Enable (D16-23)
SDRAM_DQM(3)	AA5	Data Bus Enable (D24-31)
SDRAM_DQM(4)	AA6	Data Bus Enable (D32-39)
SDRAM_DQM(5)	AA32	Data Bus Enable (D40-47)
SDRAM_DQM(6)	AB1	Data Bus Enable (D48-55)
SDRAM_DQM(7)	AB2	Data Bus Enable (D56-63)
SDRAM_RAS	AD1	Row Address Strobe
SDRAM_CAS	AD2	Column Address Strobe
SDRAM_WE#	AC1	Write Enable
SDRAM_CS1	AC2	Chip Select

Table 22. EPROM Memory Control Signal Pin Assignment

Signal	APEX Pin	Description
EPROM_CE(0)	AN8	Chip Enable
EPROM_CE(1)	AN9	Chip Enable
EPROM_OE	AD3	Output Enable

Table 23. FLASH Memory Control Signal Pin Assignment

Signal Name	APEX Pin	Description
FLASH_WE(0)	AN12	Write Enable (D0-7)
FLASH_WE(1)	AN13	Write Enable (D8-15)
FLASH_WE(2)	AN14	Write Enable (D16-23)
FLASH_WE(3)	AN15	Write Enable (D24-31)
FLASH_CS	AJ1	Chip Select
FLASH_OE	AJ2	Output Enable
FLASH_RP	AJ3	Reset/Power Down
FLASH_WP	AJ4	Write Protect

Table 24. SSRAM Bank 1 Data Bus Pin Assignment

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM1_Data(0)	B13	SSRAM1_Data(16)	B32
SSRAM1_Data(1)	B14	SSRAM1_Data(17)	B33
SSRAM1_Data(2)	B15	SSRAM1_Data(18)	C1
SSRAM1_Data(3)	B16	SSRAM1_Data(19)	C5
SSRAM1_Data(4)	B20	SSRAM1_Data(20)	C6
SSRAM1_Data(5)	B21	SSRAM1_Data(21)	C7
SSRAM1_Data(6)	B22	SSRAM1_Data(22)	C8
SSRAM1_Data(7)	B23	SSRAM1_Data(23)	C9
SSRAM1_Data(8)	B24	SSRAM1_Data(24)	C10
SSRAM1_Data(9)	B25	SSRAM1_Data(25)	C11
SSRAM1_Data(10)	B26	SSRAM1_Data(26)	C12
SSRAM1_Data(11)	B27	SSRAM1_Data(27)	C14
SSRAM1_Data(12)	B28	SSRAM1_Data(28)	C20
SSRAM1_Data(13)	B29	SSRAM1_Data(29)	C21
SSRAM1_Data(14)	B30	SSRAM1_Data(30)	C22
SSRAM1_Data(15)	B31	SSRAM1_Data(31)	C23

Table 25. SSRAM Bank 1 Address Bus Pin Assignment (Part 1 of 2)

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM1_A(0)	A2	SSRAM1_A(9)	A12
SSRAM1_A(1)	A3	SSRAM1_A(10)	A13
SSRAM1_A(2)	A4	SSRAM1_A(11)	A15
SSRAM1_A(3)	A5	SSRAM1_A(12)	A16

Table 25. SSRAM Bank 1 Address Bus Pin Assignment (Part 2 of 2)

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM1_A(4)	A6	SSRAM1_A(13)	A20
SSRAM1_A(5)	A7	SSRAM1_A(14)	A21
SSRAM1_A(6)	A9	SSRAM1_A(15)	A22
SSRAM1_A(7)	A10	SSRAM1_A(16)	A23
SSRAM1_A(8)	A11	SSRAM1_A(17)	A24

Table 26. SSRAM Bank 1 Control Signal Pin Assignment

Signal Name	APEX Pin	Direction	Description
SSRAM1_BW(0)	C24	Output	Byte Enable (D0-7)
SSRAM1_BW(1)	C25	Output	Byte Enable (D8-15)
SSRAM1_BW(2)	C26	Output	Byte Enable (B16-23)
SSRAM1_BW(3)	C27	Output	Byte Enable (D24-31)
SSRAM1_ADV	D1	Output	Address Advance
SSRAM1_ADSP	D6	Output	Address Status Processor
SSRAM1_ADSC	D7	Output	Address Status Controller
SSRAM1_OE	D8	Output	Output Enable
SSRAM1_BWE	E35	Output	Byte Write Enable
SSRAM1_GW	E34	Output	Global Write
SSRAM1_CE2	E28	Output	Chip Select
SSRAM1_CE	E27	Output	Chip Select
SSRAM1_MODE	E26	Output	Mode (select burst seq.)
SSRAM1_ZZ	E25	Output	Power Down

Table 27. SSRAM Bank 2 Data Bus Pin Assignment (Part 1 of 2)

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM2_Data(0)	D9	SSRAM2_Data(16)	D30
SSRAM2_Data(1)	D10	SSRAM1_Data(17)	D35
SSRAM2_Data(2)	D11	SSRAM2_Data(18)	E1
SSRAM2_Data(3)	D13	SSRAM2_Data(19)	E2
SSRAM2_Data(4)	D14	SSRAM2_Data(20)	E8
SSRAM2_Data(5)	D15	SSRAM2_Data(21)	E9
SSRAM2_Data(6)	D16	SSRAM2_Data(22)	E10
SSRAM2_Data(7)	D20	SSRAM2_Data(23)	E11
SSRAM2_Data(8)	D21	SSRAM2_Data(24)	E13

Table 27. SSRAM Bank 2 Data Bus Pin Assignment (Part 2 of 2)

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM2_Data(9)	D22	SSRAM2_Data(25)	E14
SSRAM2_Data(10)	D23	SSRAM2_Data(26)	E15
SSRAM2_Data(11)	D25	SSRAM2_Data(27)	E16
SSRAM2_Data(12)	D26	SSRAM2_Data(28)	E20
SSRAM2_Data(13)	D27	SSRAM2_Data(29)	E21
SSRAM2_Data(14)	D28	SSRAM2_Data(30)	E22
SSRAM2_Data(15)	D29	SSRAM1_Data(31)	E23

Table 28. SSRAM Bank 2 Address Bus Pin Assignment

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM2_A(0)	A25	SSRAM2_A(9)	A34
SSRAM2_A(1)	A26	SSRAM2_A(10)	B3
SSRAM2_A(2)	A27	SSRAM2_A(11)	B4
SSRAM2_A(3)	A28	SSRAM2_A(12)	B6
SSRAM2_A(4)	A29	SSRAM2_A(13)	B8
SSRAM2_A(5)	A30	SSRAM2_A(14)	B9
SSRAM2_A(6)	A31	SSRAM2_A(15)	B10
SSRAM2_A(7)	A32	SSRAM2_A(16)	B11
SSRAM2_A(8)	A33	SSRAM2_A(17)	B12

Table 29. SSRAM Bank 2 Control Signal Pin Assignment (Part 1 of 2)

Signal Name	APEX Pin	Direction	Description
SSRAM2_BW(0)	C28	Output	Byte Enable (D0-7)
SSRAM2_BW(1)	C29	Output	Byte Enable (D8-15)
SSRAM2_BW(2)	C30	Output	Byte Enable (B16-23)
SSRAM2_BW(3)	C31	Output	Byte Enable (D24-31)
SSRAM2_ADV	G3	Output	Address Advance
SSRAM2_ADSP	G2	Output	Address Status Processor
SSRAM2_ADSC	G1	Output	Address Status Controller
SSRAM2_OE	F34	Output	Output Enable
SSRAM2_BWE	F1	Output	Byte Write Enable
SSRAM2_GW	F2	Output	Global Write
SSRAM2_CE2	F5	Output	Chip Enable
SSRAM2_CE	F6	Output	Chip Select

Table 29. SSRAM Bank 2 Control Signal Pin Assignment (Part 2 of 2)

Signal Name	APEX Pin	Direction	Description
SSRAM2_MODE	F32	Output	Mode (select burst seq.)
SSRAM2_ZZ	F33	Output	Power Down

Table 30. RS-232 DTE Pin Assignment

Signal Name	APEX Pin	Direction	Description
DT_DTR	AG3	Output	Data Terminal Ready
DT_TD	AF34	Output	Transmit Data
DT_RTS	AG2	Output	Request to Send
DT_DCD	AE5	Input	Carrier Detect
DT_DSR	AE6	Input	Data Set Ready
DT_RD	AE34	Input	Receive Data
DT_CTS	AF1	Input	Clear To Send

Figure 4 illustrates the DTE UART interface configuration.

Figure 4. DTE UART Interface

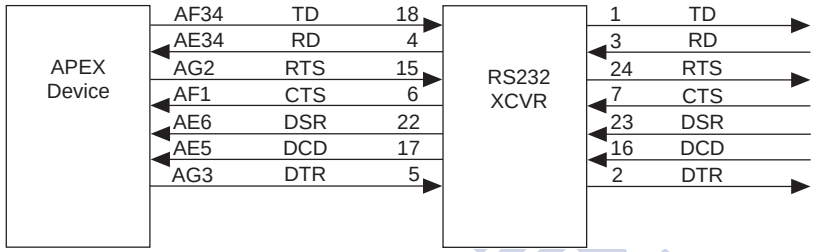


Table 31. RS-232 DCE Pin Assignment

Signal Name	APEX Pin	Direction	Description
DC_DTR	AF4	Input	Data Terminal Ready
DC_TD	AF2	Input	Transmit Data
DC_RTS	AF3	Input	Request to Send
DC_DCD	AG6	Output	Carrier Detect
DC_DSR	AG30	Output	Data Set Ready
DC_RD	AG35	Output	Receive Data
DC_CTS	AC33	Output	Clear To Send
DC_DTR	AF4	Input	Data Terminal Ready

Figure 5 illustrates the DCE UART interface.

Figure 5. DCE UART Interface

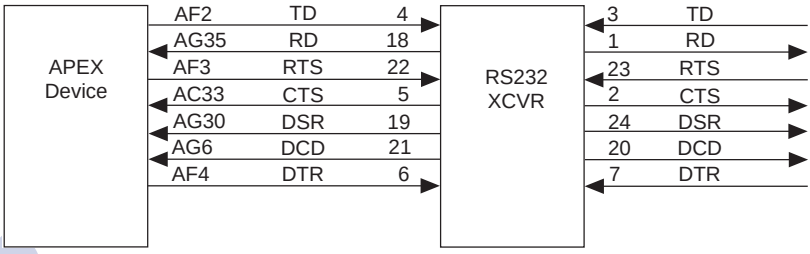


Table 32. PS/2 Keyboard Pin Assignment

Signal Name	APEX Pin	Direction	Description
K_DATA_OUT	B5	Output	Output Data
K_DATA_IN	G31	Input	Input Data
K_CLK_OUT	B7	Output	Output Data Clock
K_CLK_IN	G6	Input	Input Data Clock

Figure 6. Keyboard & Mouse Interface

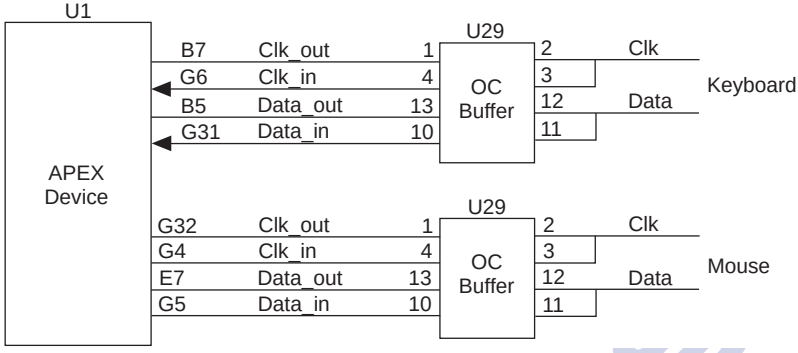


Table 33. PS/2 Mouse Pin Assignment

Signal Name	APEX Pin	Direction	Description
M_DATA_OUT	E7	Output	Output Data
M_DATA_IN	G5	Input	Input Data
M_CLK_OUT	G32	Output	Output Data Clock
M_CLK_IN	G4	Input	Input Data Clock

Table 34. USB Pin Assignment

Signal Name	APEX Pin	Direction	Description
USB_OE	J4	Output	USB Transceiver Enable
USB_SUSPND	J5	Output	Suspend (Low power mode)
USB_SPEED	J6	Output	Edge Rate Speed Control
USB_VPO	P5	Output	Output Data from SIE
USB_VMO	P6	Output	Output Data from SIE
USB_RCV	G33	Input	Receive Data input to SIE
USB_VP	H6	Input	Gated Version of D+
USB_VM	J1	Input	Gated Version of D-
USB_RERR	J2	Input	Receive Error
USB_RSEO	J3	Input	Receive Single Ended Zero

Figure 7 illustrates the USB interface.

Figure 7. USB Interface

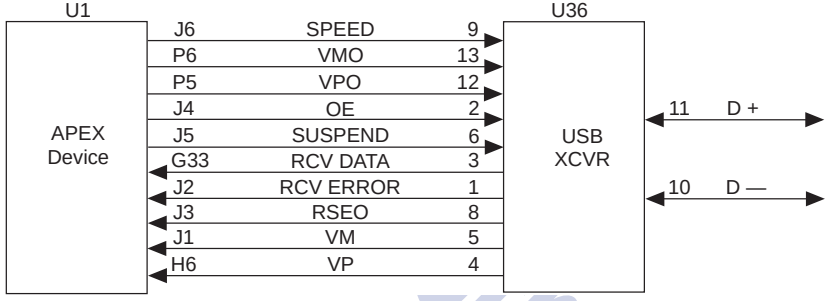


Table 35. IEEE-1394 Interface Pin Assignment (Part 1 of 2)

Signal Name	APEX Pin	Direction	Description
FW_DATA(0)	AJ6	Input/Output	Fire Wire Data (0)
FW_DATA(1)	AK1	Input/Output	Fire Wire Data (1)
FW_DATA(2)	AK3	Input/Output	Fire Wire Data (2)
FW_DATA(3)	AK4	Input/Output	Fire Wire Data (3)
FW_DATA(4)	AK5	Input/Output	Fire Wire Data (4)
FW_DATA(5)	AL1	Input/Output	Fire Wire Data (5)
FW_DATA(6)	AL9	Input/Output	Fire Wire Data (6)
FW_DATA(7)	AL10	Input/Output	Fire Wire Data (7)
FW_RESET	AF6	Output	Reset

Table 35. IEEE-1394 Interface Pin Assignment (Part 2 of 2)

Signal Name	APEX Pin	Direction	Description
FW_LREQ	AK2	Input	Link Request (to LLC)
FW_PD	AL11	Output	Power Down
FW_CTL0	AL13	Output	Control 0
FW_CTL1	AL14	Output	Control 1
FW_CNA	AL15	Output	Cable Not Active output
FW_LKON	AL7	Input	Link On (Connected)

Figure 8 illustrates the IEEE 1394 Firewire interface.

Figure 8. IEEE 1394 Firewire Interface

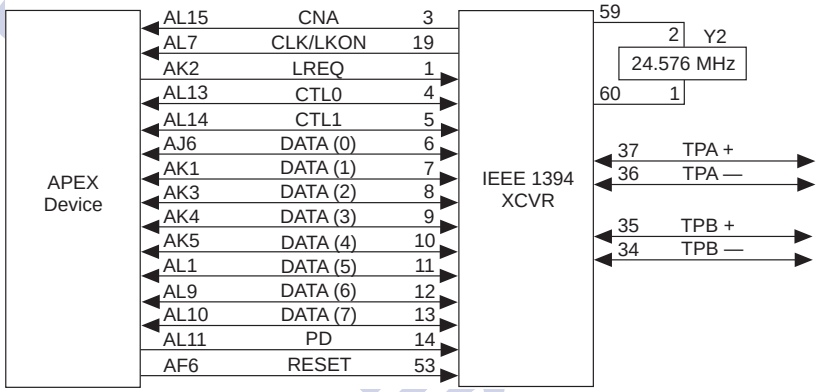


Table 36. Ethernet Interface Pin Assignment (Part 1 of 2)

Signal Name	APEX Pin	Direction	Description
ETH_TXD(0)	J30	Output	Transmit Data (0)
ETH_TXD(1)	J31	Output	Transmit Data (1)
ETH_TXD(2)	J32	Output	Transmit Data (2)
ETH_TXD(3)	J33	Output	Transmit Data (3)
ETH_TX_EN	J35	Output	Transmit Enable
ETH_TX_ER	J34	Output	Transmit Error
ETH_MDC	M6	Output	Management Data Clock
ETH_GLOB_RES	A8	Output	Reset
ETH_RX_DV	AH6	Input	Receive Data Valid
ETH_RX_ER	AJ5	Input	Receive Error

Table 36. Ethernet Interface Pin Assignment (Part 2 of 2)

Signal Name	APEX Pin	Direction	Description
ETH_RXD(0)	AH1	Input	Receive Data
ETH_RXD(1)	AH2	Input	Receive Data
ETH_RXD(2)	AH3	Input	Receive Data
ETH_RXD(3)	AH5	Input	Receive Data
ETH_MDIO	AK6	Input/Output	Management Data I/O
ETH_COL	Y31	Input	Collision
ETH_INTR	AK35	Input	Interrupt
ETH_CRS	R1	Input	Carrier Sense

Figure 9 illustrates the ethernet interface.

Figure 9. Ethernet Interface

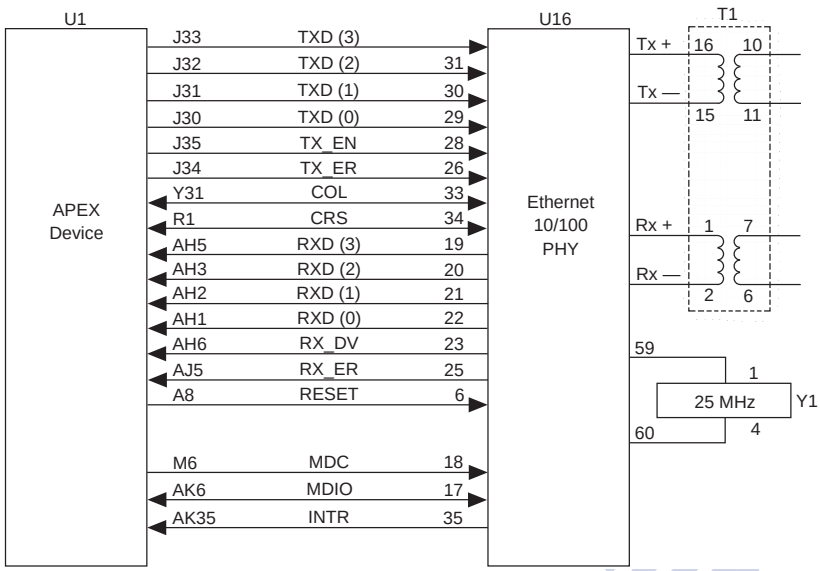


Table 37. Parallel Port Interface in Host Mode (Part 1 of 2)

Signal Name	APEX Pin	Direction	Description
PP_D(0)	AM1	Input/Output	Bi-directional Data line
PP_D(1)	AM6	Input/Output	Bi-directional Data line
PP_D(2)	AM7	Input/Output	Bi-directional Data line
PP_D(3)	AM8	Input/Output	Bi-directional Data line

Table 37. Parallel Port Interface in Host Mode (Part 2 of 2)

Signal Name	APEX Pin	Direction	Description
PP_D(4)	AM9	Input/Output	Bi-directional Data line
PP_D(5)	AM10	Input/Output	Bi-directional Data line
PP_D(6)	AM11	Input/Output	Bi-directional Data line
PP_D(7)	AM13	Input/Output	Bi-directional Data line
PP_SLCTIN_N	AL16	Output	Deselect Protocol
PP_INT_N	AL20	Output	Initialize Printer
PP_AFEED_N	AL21	Output	Auto Feed
PP_STROBE_N	AL22	Output	Data Strobe
PP_HD	AL23	Output	HD Enable
PP_DIR	AL27	Output	Control Direction of Data
PP_ACK_N	AM14	Input	Finished with last char
PP_BUSY	AM15	Input	Not Ready
PP_PEND	AM16	Input	Paper End
PP_SLCT	AM20	Input	Select
PP_ERR_N	AM21	Input	Error (Cannot Print)

Figure 10 illustrates the parallel port interface in host mode.

Figure 10. Parallel Port Interface in Host Mode

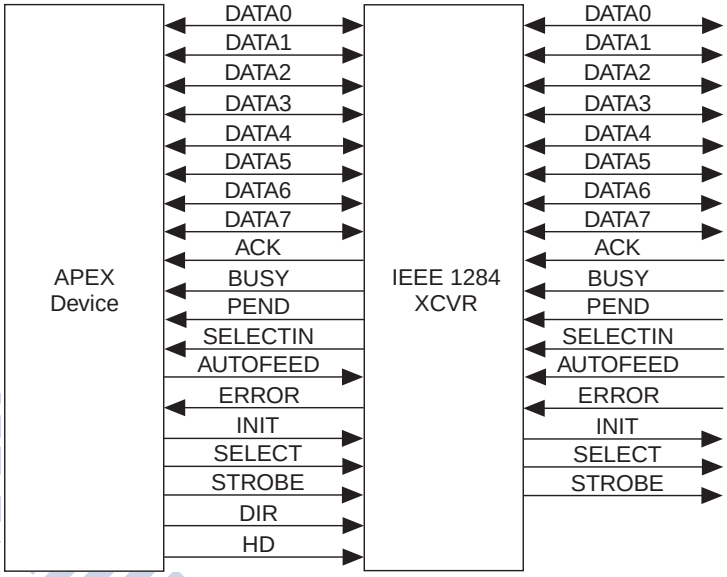


Table 38. Parallel Port Interface in Peripheral Mode

Signal Name	APEX Pin	Direction	Description
PP_D(0)	AM1	Input/Output	Bidirectional Data Line
PP_D(1)	AM6	Input/Output	Bidirectional Data Line
PP_D(2)	AM7	Input/Output	Bidirectional Data Line
PP_D(3)	AM8	Input/Output	Bidirectional Data Line
PP_D(4)	AM9	Input/Output	Bidirectional Data Line
PP_D(5)	AM10	Input/Output	Bidirectional Data Line
PP_D(6)	AM11	Input/Output	Bidirectional Data Line
PP_D(7)	AM13	Input/Output	Bidirectional Data Line
PP_BUSY	AL16	Output	Not Ready
PP_ACK_N	AL20	Output	Ready For Next Char
PP_ERR_N	AL21	Output	Error (Cannot Print)
PP_PEND	AL22	Output	Paper End
PP_HD	AL23	Output	HD enable
PP_DIR	AL27	Output	Control Direction of Data
PP_INIT_N	AM14	Input	Initialize Printer
PP_SLCTIN_N	AM15	Input	Deselect Protocol
PP_STROB	AM16	Input	Data Strobe
PP_SLCT	AM20	Input	Select
PP_AFEED	AM21	Input	Auto Feed

Table 39. EJTAG Interface Pin Assignment

Signal Name	APEX Pin	Direction
EJTAG_TRST	AB3	Input/Output
EJTAG_TDI	AB4	Input/Output
EJTAG_TDO	C13	Input/Output
EJTAG_TMS	AB5	Input/Output
EJTAG_TCK	AB32	Input/Output
EJTAG_RST	AD4	Input/Output
EJTAG_PCST[0]	AD5	Input/Output
EJTAG_PCST[1]	AD6	Input/Output
EJTAG_PCST[2]	AD33	Input/Output
EJTAG_DCLK	AE1	Input/Output
EJTAG_PCST2[0]	AE4	Input/Output
EJTAG_TPC2	AE3	Input/Output
EJTAG_PCST2[1]	N32	Input/Output
EJTAG_PCST2[2]	N33	Input/Output
EJTAG_TPC3	R6	Input/Output
EJTAG_PCST3[0]	T1	Input/Output
EJTAG_PCST3[1]	N34	Input/Output
EJTAG_PCST3[2]	T3	Input/Output
EJTAG_TPC4	P31	Input/Output
EJTAG_PCST4[0]	T5	Input/Output
EJTAG_PCST4[1]	W5	Input/Output
EJTAG_PCST4[2]	P30	Input/Output
EJTAG_TPC5	P33	Input/Output
EJTAG_TPC6	P34	Input/Output
EJTAG_TPC7	Y4	Input/Output
EJTAG_TPC8	Y6	Input/Output

PMC Interface

Tables 40 through 42 provide pin definitions for the three connectors of the PMC interface. The PMC connector pins are allocated as specified in the PMC specification and the PMC Mezzanine sections.

Table 40. PMC Interface JN1 Pin Assignments

Signal Name	APEX Pin	PMC Pin
PMC_INTA#	T35	JN1-4
PMC_INTB#	H2	JN1-5
PMC_INTC#	H3	JN1-6
PMC_INTD#	H4	JN1-9
PMC_GNT#	AM29	JN1-16
PMC_REQ#	AL29	JN1-17
AD(31)	AR31	JN1-20
AD(28)	AR32	JN1-21
AD(27)	AP32	JN1-22
AD(25)	AP33	JN1-23
PMC_C_BE(3)	AM25	JN1-26
AD(22)	AL33	JN1-27
AD(21)	AL35	JN1-28
AD(19)	AK31	JN1-29
AD(17)	AK34	JN1-32
PMC_FRAME#	AM27	JN1-33
PMC_IRDY#	AP17	JN1-36
PMC_DEVSEL#	AN29	JN1-37
PMC_LOCK#	L1	JN1-40
PMC_SDONE	AJ33	JN1-41
PMC_SBO	AL8	JN1-42
PMC_PAR	AR30	JN1-43
AD(15)	AJ31	JN1-46
AD(12)	AJ35	JN1-47
AD(11)	AH30	JN1-48
AD(9)	AH33	JN1-49
PMC_C_BE(0)	AM26	JN1-52
AD(6)	AG32	JN1-53
AD(5)	AG33	JN1-54
AD(4)	AG34	JN1-55
AD(3)	AF30	JN1-58
AD(2)	AF31	JN1-59
AD(1)	AF32	JN1-60
AD(0)	AF33	JN1-61
PMC_REQ64#	AN30	JN1-64

Table 41. PMC Interface JN2 Pin Assignment

Signal Name	APEX Pin	PMC Pin
PMC_GLOB_RES	L6	JN2-13
AD(30)	AP31	JN2-19
AD(29)	AN31	JN2-20
AD(26)	AR33	JN2-22
AD(24)	AR34	JN2-23
PMC_IDSEL	AL34	JN2-25
AD(23)	AM35	JN2-26
AD(20)	AK30	JN2-28
AD(18)	AK32	JN2-29
AD(16)	AJ30	JN2-31
PMC_C_BE(2)	AL25	JN2-32
PMC_TRDY#	AP19	JN2-35
PMC_STOP#	AP30	JN2-38
PMC_PERR#	AR29	JN2-39
PMC_SERR#	AP29	JN2-42
PMC_C_BE(1)	AN26	JN2-43
AD(14)	AJ32	JN2-45
AD(13)	AJ34	JN2-46
AD(10)	AH32	JN2-48
AD(8)	AH34	JN2-49
AD(7)	AG31	JN2-51

Table 42. PMC Interface JN3 Pin Assignments (Part 1 of 2)

Signal Name	APEX Pin	PMC Pin
PMC_C_BE(7)	AL26	JN3-4
PMC_C_BE(6)	AP27	JN3-5
PMC_C_BE(5)	AN27	JN3-6
PMC_C_BE(4)	AP28	JN3-7
PMC_PAR64	AN28	JN3-10
AD(63)	AF35	JN3-11
AD(62)	AE30	JN3-12
AD(61)	AE31	JN3-13
AD(60)	AE32	JN3-16
AD(59)	AE35	JN3-17
AD(58)	AD30	JN3-18

Table 42. PMC Interface JN3 Pin Assignments (Part 2 of 2)

Signal Name	APEX Pin	PMC Pin
AD(57)	AD31	JN3-19
AD(56)	AD32	JN3-22
AD(55)	AD34	JN3-23
AD(54)	AD35	JN3-24
AD(53)	AC30	JN3-25
AD(52)	AC31	JN3-28
AD(51)	AC34	JN3-29
AD(50)	AC35	JN3-30
AD(49)	AB30	JN3-31
AD(48)	AB31	JN3-34
AD(47)	AB33	JN3-35
AD(46)	AB34	JN3-36
AD(45)	AB35	JN3-37
AD(44)	R30	JN3-40
AD(43)	AA33	JN3-41
AD(42)	AA34	JN3-42
AD(41)	T32	JN3-43
AD(40)	T30	JN3-46
AD(39)	P32	JN3-47
AD(38)	Y33	JN3-48
AD(37)	P35	JN3-49
AD(36)	Y35	JN3-52
AD(35)	R32	JN3-53
AD(34)	R33	JN3-54
AD(33)	T31	JN3-55
AD(32)	R35	JN3-58

Table 43. General-Purpose Mezzanine Interface J3 Pin Assignments

Signal Name	APEX Pin	GP Mezzanine Connector Pin
GP_IO(0)	K30	J3-1
GP_IO(1)	K32	J3-5
GP_IO(2)	K33	J3-7
GP_IO(3)	K34	J3-9
GP_IO(4)	K35	J3-13
GP_IO(5)	L30	J3-17

Table 43. General-Purpose Mezzanine Interface J3 Pin Assignments

Signal Name	APEX Pin	GP Mezzanine Connector Pin
GP_IO(6)	L31	J3-19
GP_IO(7)	L32	J3-21
GP_IO(8)	L33	J3-23
GP_IO(9)	L34	J3-27
GP_IO(10)	L35	J3-29
GP_IO(11)	M31	J3-31
GP_IO(12)	M32	J3-33
GP_IO(13)	M33	J3-37
GP_IO(14)	M34	J3-41
GP_IO(15)	M35	J3-43
GP_IO(16)	N30	J3-45
GP_IO(17)	H34	J3-47
GP_IO(18)	H35	J3-49
GP_IO(19)	M1	J3-53
GP_IO(20)	N1	J3-55
GP_IO(21)	P2	J3-57
GP_IO(22)	R2	J3-59
GP_IO(23)	A14	J3-61
GP_IO(24)	C15	J3-4
GP_IO(29)	L2	J3-10

Table 44. General-Purpose Mezzanine J2 Pin Assignments (Part 1 of 2)

Signal Name	APEX Pin	GP Mezzanine Connector Pin
GP_IO(25)	H30	J2-3
GP_IO(26)	H31	J2-5
GP_IO(27)	H32	J2-9
GP_IO(28)	H33	J2-11
GP_MEZZ_RST	AG4	J2-13
GP_IO(30)	K3	J2-17
GP_IO(31)	K4	J2-19
GP_IO(32)	K5	J2-23
GP_IO(33)	K6	J2-25
GP_IO(34)	AL28	J2-29
GP_IO(35)	AM28	J2-31

Table 44. General-Purpose Mezzanine J2 Pin Assignments (Part 2 of 2)

Signal Name	APEX Pin	GP Mezzanine Connector Pin
GP_IO(36)	G34	J2-35
GP_IO(37)	G35	J2-39
CLKOUT0	U31	J2-43
CLKOUT1	Y3	J2-49
CLKFBIN0	Y32	J2-45
CLKFBIN1	T4	J2-51

Table 45. VGA Interface Pin Assignments

Signal Name	APEX Pin	Description
VSYNC	AM22	Vertical Synchronization
HSYNC	AM23	Horizontal Synchronization
BLUE	AN5	Blue Signal Output
GREEN	AN6	Green Signal Output
RED	AN7	Red Signal Output

Table 46. LCD Interface Pin Assignments

Signal Name	APEX Pin	Description
LCD_DB(0)	M2	Data signal (LSB)
LCD_DB(1)	M3	Data signal
LCD_DB(2)	M4	Data signal
LCD_DB(3)	M5	Data signal
LCD_DB(4)	N2	Data signal
LCD_DB(5)	N3	Data signal
LCD_DB(6)	N5	Data signal
LCD_DB(7)	N6	Data signal (MSB)
LCD_RS	P1	Register Select
LCD_RW	P3	Read / not Write signal
LCD_ENABLE	P4	Enable signal

Table 47. LED & Switch Pin Assignment		
Signal Name	**APEX Pin**	**Description**
LOCK1/LED 4	AA30	Active hi lock 1 / User LED
LOCK2/LED 3	AB6	Active hi lock 2 / User LED
LOCK3 / LED 2	R31	Active hi lock 3 / User LED
LOCK4 / LED 1	AC6	Active hi lock 4 / User LED
APEX_LED5	K2	User LED 5 (Active Low)
APEX_LED6	K1	User LED 6 (Active Low)
GLOB_RES	T6	Global Device Clear Input
APEX_SW2	B17	Low Skew Reset
APEX_SW3	L4	User switch
APEX_SW4	L5	User switch

Connector Pin Assignments

For the connectors on the board, the pin numbering is indicated on the board.

JTAG / MasterBlaster Configuration Header

The MasterBlaster cable header is a 2 × 5 0.1 inch header used to connect the MasterBlaster cable to the board. The reference designator for the header is JP12.

Table 48. JTAG/MasterBlaster Header Pin Definition	
Pin	**Signal Name**
1	MASTER_TCK
2	GND
3	MASTER_TDO
4	VCC (3.3 V)
5	MASTER_TMS
6	VIO (3.3 V)
7	N/C
8	N/C
9	MASTER_TDI
10	GND

EJTAG Connector

The EJTAG connector is a 2 × 26 pin 0.050 inch header. The reference designator for the header is J10. Table 49 only lists the odd pins because all of the even-numbered pins are connected to ground.

Table 49. EJTAG Connector Pin Definition

Pin	Signal Name
1	EJTAG_TRST
3	EJTAG_TDI
5	EJTAG_TDO
7	EJTAG_TMS
9	EJTAG_TCK
11	EJTAG_RST*
13	EJTAG_PCST[0]
15	EJTAG_PCST[1]
17	EJTAG_PCST[2]
19	EJTAG_DCLK
21	EJTAG_TRC2
23	EJTAG_PCST2[0]
25	EJTAG_PCST2[1]
27	EJTAG_PCST2[2]
29	EJTAG_TPC3
31	EJTAG_PCST3[0]
33	EJTAG_PCST3[1]
35	EJTAG_PCST3[2]
37	EJTAG_TPC4
39	EJTAG_PCST4[0]
41	EJTAG_PCST4[1]
43	EJTAG_PCST4[2]
45	EJTAG_TPC5
47	EJTAG_TPC6
49	EJTAG_TPC7
51	EJTAG_TPC8

RS-232 DTE Connector

Table 50 lists the RS-232C DTE interface connector pin-out. The RS-232C DTE is a DB9 female connector. The reference designator for this connector is J12.

Table 50. RS-232C DTE Connector Definition

Pin	Signal Name	Input/Output
1	DCD	Input
2	RD	Input
3	TD	Output
4	DTR	Output
5	GND	
6	DSR	Input
7	RTS	Output
8	CTS	Input
9	N/C	

RS-232 DCE Connector

Table 51 lists the pin out for the RS-232C DCE interface connector. The RS-232C DCE connector is a DB9 male receptacle. The reference designator for this connector is J13.

Table 51. RS-232C DCE Connector Definition

Pin	Signal Name	Input/Output
1	DCD	Output
2	RD	Output
3	TD	Input
4	DTR	Input
5	GND	
6	DSR	Output
7	RTS	Input
8	CTS	Output
9	N/C	

PS/2 Connectors

Table 52 lists the PS/2 pin-outs. These pin-outs are the same for both the J17 and J18 connectors. Table 52 lists the connector pin definitions for both PS/2 connectors.

Table 52. PS/2 Connector Definition

Pin	Signal Name	Input/Output
1	DATA	Input/Output
2	N/C	
3	GND	
4	5 V	
5	CLOCK	Input/Output
6	N/C	

USB Connector

The USB connector is J16. Table 53 lists the connector pin definitions.

Table 53. USB Connector Definition

Pin	Signal Name	Input/Output
1	Optional Power*	Output
2	D-	Input/Output
3	D+	Input/Output
4	GND	Output

If the downstream device requires power, it may be provided by installing JP20. Be sure to remove this jumper if power is not required.

IEEE-1394 (Firewire) Connector

The Firewire connector is J15, and the connector pin definition is listed in Table 54.

Table 54. IEEE-1394a Connector Definition		
Pin	**Signal Name**	**Input/Output**
1	CPS	Input
2	GND	
3	TPB0-	Input/Output
4	TPB0+	Input/Output
5	TPA0-	Input/Output
6	TPA0+	Input/Output

Ethernet Connector

The Ethernet connector is J11. Table 55 lists the connector pin definitions.

Table 55. Ethernet Connector Definition		
Pin	**Signal Name**	**Input / Output**
1	TX+	Output
2	TX-	Output
3	RX+	Input
4	N/C	Input
5	N/C	
6	RX-	Output
7	N/C	Input
8	N/C	Output

Parallel Port Connector

The IEEE-1284 (Parallel Port) interface connector is J14 and is a DB25 female connector. The connector pin definitions are listed in Table 56.

Table 56. Parallel Port Connector Definition (Part 1 of 2)		
Pin	**Signal Name**	**Input / Output**
1	STROBE	Output
2	D(0)	Input/Output
3	D(1)	Input/Output
4	D(2)	Input/Output
5	D(3)	Input/Output
6	D(4)	Input/Output

Table 56. Parallel Port Connector Definition (Part 2 of 2)

Pin	Signal Name	Input / Output
7	D(5)	Input/Output
8	D(6)	Input/Output
9	D(7)	Input/Output
10	ACKNLG	Input
11	BUSY	Input
12	PEND	Input
13	SLCT	Input
14	AFEED	Output
15	ERROR	Input
16	INIT	Output
17	SLCT	Output
18	GND	
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	
25	GND	

VGA Connector

The VGA Connector is J9, and is a DB15 male connector. Table 57 lists the connector pin definitions.

Table 57. VGA Connector Definition (Part 1 of 2)

Pin	Signal Name	Input / Output
1	RED	Output
2	GREEN	Output
3	BLUE	Output
4	N/C	
5	GND	
6	GND	
7	GND	
8	GND	
9	N/C	

Table 57. VGA Connector Definition (Part 2 of 2)		
Pin	**Signal Name**	**Input / Output**
10	GND	
11	N/C	
12	N/C	
13	HSYNC	Output
14	VSYNC	Output
15	N/C	

Test Connectors

This section lists the pins connected to each of the six logic analyzer test connectors on the board. These connectors are not in use, but the signals are connected as listed in Tables 58 through 63. These signals may be used by populating the required connector or probing directly on the connector pads.

Table 58. JP5 Pin Definition	
Pin	**Signal Name**
1	N/C
2	N/C
3	N/C
4	GPM_DATA[7]
5	GPM_DATA[6]
6	GPM_DATA[5]
7	GPM_DATA[4]
8	GPM_DATA[3]
9	GPM_DATA[2]
10	GPM_DATA[1]
11	GPM_DATA[0]
12	GPM_ADDRESS[7]
13	GPM_ADDRESS[6]
14	GPM_ADDRESS[5]
15	GPM_ADDRESS[4]
16	GPM_ADDRESS[3]
17	GPM_ADDRESS[2]
18	GPM_ADDRESS[1]
19	GPM_ADDRESS[0]
20	GND

Table 59. JP3Pin Definition

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SSRAM2_D[7]
5	SSRAM2_D[6]
6	SSRAM2_D[5]
7	SSRAM2_D[4]
8	SSRAM2_D[3]
9	SSRAM2_D[2]
10	SSRAM2_D[1]
11	SSRAM2_D[0]
12	SSRAM2_A[7]
13	SSRAM2_A[6]
14	SSRAM2_A[5]
15	SSRAM2_A[4]
16	SSRAM2_A[3]
17	SSRAM2_A[2]
18	SSRAM2_A[1]
19	SSRAM2_A[0]
20	GND

Table 60. JP2 Pin Definition (Part 1 of 2)

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SSRAM1_D[7]
5	SSRAM1_D[6]
6	SSRAM1_D[5]
7	SSRAM1_D[4]
8	SSRAM1_D[3]
9	SSRAM1_D[2]
10	SSRAM1_D[1]
11	SSRAM1_D[0]
12	SSRAM1_A[7]
13	SSRAM1_A[6]

Table 60. JP2 Pin Definition (Part 2 of 2)

Pin	Signal Name
14	SSRAM1_A[5]
15	SSRAM1_A[4]
16	SSRAM1_A[3]
17	SSRAM1_A[2]
18	SSRAM1_A[1]
19	SSRAM1_A[0]
20	GND

Table 61. JP1 Pin Definition

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SSRAM1_BWE[3]
5	SSRAM1_BWE[2]
6	SSRAM1_BWE[1]
7	SSRAM1_BWE[0]
8	SSRAM1_ADV#
9	SSRAM1_ADSP#
10	SSRAM1_ADSC#
11	SSRAM1_OE#
12	SSRAM1_BWE#
13	SSRAM1_GW#
14	SSRAM1_CE2
15	SSRAM1_CE#
16	FLASH_WE[3]
17	FLASH_WE[2]
18	FLASH_WE[1]
19	FLASH_WE[0]
20	GND

Table 62. JP4 Pin Definition

Pin	Signal Name
1	N/C
2	N/C
3	TEST_CLK
4	FLASH_RP#
5	FLASH_OE#
6	SSRAM2_BWE[3]
7	SSRAM2_BWE[2]
8	SSRAM2_BWE[1]
9	SSRAM2_BWE[0]
10	SSRAM2_ADV#
11	SSRAM2_ADSP#
12	SSRAM2_ADSC#
13	SSRAM2_OE#
14	SSRAM2_BWE#
15	SSRAM2_GW#
16	SSRAM2_CE2
17	SSRAM2_CE#
18	FLASH_CS#
19	TEST_CLK
20	GND

Table 63. JP6 Pin Definition (Part 1 of 2)

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SDRAM_CS2#
5	SDRAM_RAS#
6	EPROM_CE2#
7	SDRAM_CS1#
8	EPROM_CE1#
9	SDRAM_CAS#
10	EPROM_OE
11	SDRAM_WE#
12	SDRAM_DQM[7]

Table 63. JP6 Pin Definition (Part 2 of 2)

Pin	Signal Name
13	SDRAM_DQM[6]
14	SDRAM_DQM[5]
15	SDRAM_DQM[4]
16	SDRAM_DQM[3]
17	SDRAM_DQM[2]
18	SDRAM_DQM[1]
19	SDRAM_DQM[0]
20	GND

General Usage Guidelines

To ensure proper use of the development board and to avoid damage to the board, you should follow the guidelines in this section.

SDRAM Data Bus

The SDRAM data bus is 64-bits wide and the general-purpose memory data bus is only 32-bits wide. To allow all of the SDRAM memory array to be accessed, the data bus is doubled, which means that the lower half of the SDRAM data pins on the DIMM are directly connected to the upper half. For example, data pins 0 and 32 on the DIMM are connected to general-purpose memory data bus pin 0. Only one of these pins can be active at one time. The output from the SDRAM is controlled by the DQM[7..0] lines; ensure that only the desired portion of the bus is enabled at any one time.

Parallel Port Jumpers

Nine jumpers were added to the development board to allow the parallel port to operate in both host and peripheral mode. The jumpers switch the direction of the control lines depending on which mode is desired. Ensure that all of the jumpers are in the same position. All jumpers must be shorting pins 1 and 2 for the port to be in host mode. All jumpers must be shorting pins 2 and 3 for the port to be in peripheral mode. Any other configuration will cause contention and the parallel port will not function properly.

Unused APEX Device Pins

All general-purpose I/O APEX device pins have been allocated for on-board functions. In most circumstances, not all of the pins will be required to be active. It is very important that if a pin is not used, that it be left in the high impendence (input) state. This will avoid unnecessary power consumption and possible contention. All the critical control lines for the interfaces on the board are pulled to the inactive state. If a device is not used, it can be ignored and the APEX device interface pins left as inputs.

Power Consumption

This is only applicable if the board is powered from the terminal strip and not the supply. Altera recommends that you monitor the input current to be sure that the power being supplied is sufficient. The power required by the board is directly related to the following:

- The Amount of Interfaces used.
- The Density and Speed of the APEX.
- Population of either Mezzanine.

The typical maximum current is 5 Amps. This can be exceeded if the board is heavily loaded with many interfaces running at a high-clock speed.

Testing Software

The development board includes test cores to help developers perform functional tests on cores.

Test Core Functionality

For implementing a test plan, multiple test cores are included with the development board and can be programmed onto the APEX device using the JTAG chain. Each test core tests one or more interface and uses LEDs to a pass or a fail a design.

Table 64 lists test cores are available to test the SOPC Development Board.

Table 64. Test Cores Available for the Development Board

Test Core Name	Test Interface
Mix_Test_1.sof	-Configuration of the APEX device -Switches and LED interface -VGA interface
Mix_Test_2.sof	-SRAM1 interface -SRAM2 interface
Mix_Test_3.sof	-RS232 interface -PS2 interface -USB interface -Parallel interface -PMC interface -GPM interface -EJTAG interface -JTAG chain
Mix_Test_4.sof	-FireWire interface -Ethernet interface
Mix_Test_5.sof	-Flash interface -Eprom interface
Sdram_top.sof	-SDRAM interface
Lcd_top.pof **Lcd_top1.pof** **Lcd_top2.pof**	-LCD interface -EPC2s

Mix_Test_1 Core

The Mix_Test_1 Core performs a test on the configuration interface, the switches and LED interface, and the VGA interface.

Switch & LED Test

The configuration interface test confirms the proper operation of the configuration circuitry of the APEX device. The APEX device is first configured directly using the MasterBlaster cable with the Mix_Test_1 test core, **Mix_Test_1.sof**. Proper configuration of the APEX device indicates proper functioning of the configuration interface.

The switches and LED interface test confirms the proper operation of the user switches and LEDs. The test core allows the LEDs to be turned on and off by the user switches, confirming the proper operation of both the switches and the LEDs. During reset, all the LEDs are illuminated. Pressing another switche causes two of the LEDs to turn on.

Table 65. User Switch & LED Test

User Switch	User LEDs
S2	LED11, LED12
S3	LED13, LED14
S4	LED15, LED16

VGA Interface Test

The VGA interface test confirms the proper operation of the VGA interface. The core provides an output waveform, a "walking one's" pattern to the five outputs, to the VGA connector that is measured using an oscilloscope to confirm proper operation. The proper LVTTL logic levels are confirmed for the sync signals while the color signals are verified to be within the acceptable analog level, 0.5 to 0.7 V. The presence and timing of the pulse waveform verifies the proper connection of the VGA signals. A pulse width greater than a clock period, 40 ns, or multiple pulses occurring within a five clock period time frame signify a failed test result.

Mix_Test_2 Core

The Mix_Test_2 Core confirms the proper operation of both SSRAM memories operating at 66 MHz. Both reads and writes are performed to each device including 32-bit accesses and 8-bit cycles to test the byte lane control signals and burst accesses. In addition, the address and data convergence testing of the SSRAM buses are completed. The address convergence test is performed first, using 32-bit accesses. The test writes a unique value to all addresses and reads each memory location to ensure the presence of the correct data. The core then checks the integrity of the data bus by writing a "walking one's and zero's" pattern to the SSRAM. All values are read back and checked. The core performs a 32-bit burst write of length four followed by four 32-bit reads to verify the data. Two 16-bit writes are followed by a single 32-bit read for verification of the data. Finally, a single 32-bit write is confirmed by four 8-bit reads.

Table 66 lists the error detection codes used to identify an interface that failed a test. LEDs D[14..11] are used to display this error detection code.

Table 66. Error Detection Codes

SRAM Core	Error LED	Done LED
SRAM1 core	D11	D13
SRAM2 core	D12	D14

Mix_Test_3 Core

The Mix_Test_3 performs a variety of test including:

- RS-232 Interface
- PS/2 Interface
- USB Interface
- IEEE 1284 Interface
- PMC-PCI Interface
- General-Purpose MezzanineInterface
- EJTAG Interface
- JTAG Interface

RS-232 Interface

This test confirms the proper operation of the RS-232 interface. The core provides a "walking one's and zero's" pattern to the RS-232 outputs. The outputs of each connector are wired to the inputs of the other connector. The inputs are read to check for the proper pattern on the outputs of each interface.

PS/2 Interface

This test confirms the proper operation of the PS/2 interface. The core provides a "walking one's and zero's" pattern to the PS/2 connectors that are wired from one connector to the other. The inputs are read to check for the proper pattern on the outputs of each interface.

Universal Serial Bus (USB) Interface

This test confirms the proper operation of the USB interface. The core provides an output waveform to the USB connector that is measured using an oscilloscope to confirm proper operation. A data pattern of `10101100` is transmitted at the 12 MHz data rate. The input signals from the USB transceiver are also checked to confirm they remain at a low LVTTL logic level.

IEEE 1284 Parallel Interface

This test confirms the proper operation of the Parallel interface. The four sub-cores provide a "walking one's and zero's" pattern to the parallel connector that has the various outputs wired to the available inputs. The inputs are read to check for the proper pattern on the outputs of each interface. Multiple cores and connectors are required to cover all the available outputs with the limited number of inputs.

PMC - PCI Interface

This test confirms the proper operation of the PMC interface. The core provides a "walking one's and zero's" pattern to the PMC connectors that are wired from the designated outputs to the inputs. The inputs are read to check for the proper pattern on the outputs of each interface. This core is run at 66 Mhz to ensure that PCI interface can support operation at this frequency.

General-Purpose Mezzanine Interface

This test confirms the proper operation of the General-Purpose Mezzanine interface. The core provides a "walking one's and zero's" pattern to the GPM connectors that are wired from one connector to the other. The inputs are read to check for the proper pattern on the outputs of each interface.

EJTAG Interface

This test confirms the proper operation of the EJTAG interface. The core provides a "walking one's and zeros" pattern to the EJTAG connector that is wired from outputs to inputs. The inputs are read to check for the proper pattern on the outputs of each interface.

JTAG Interface

This test confirms the proper operation of the JTAG interface. The JTAG chain is configured to include the APEX device, PMC, and general-purpose mezzanine. The cables on the PMC and general-purpose mezzanine connectors connect the `TDI` signal to `TDO` allowing the APEX device to be programmed if the chain is functional. The Mix_Test_3 core, **Mix_Test_3.sof** is programmed onto the APEX device.

The following error detection code is used to identify an interface that failed the test. LEDs `D[16..14]` are used to display this error detection code.

Table 67. Mix_Test_3 Error Detection Codes *Note (1)*

Interface	D14	D15	D16
No failure	0	0	0
RS232	0	0	1
EJTAG	0	1	0
General-purpose mezzanine	0	1	1
Parallel	1	0	0
PMC	1	0	1
PS2	1	1	0
USB	1	1	1

Note:
(1) A one (1) indicates illuminated, and a zero (0) indicates not illuminated.

Mix_Test_4

The Mix_Test_4 performs tests on the IEEE 1394 and 10/100BASE-TX Ethernet interfaces.

IEEE 1394 (Firewire) Interface

This test confirms the proper operation of the Firewire interface. The core performs read and write cycles to registers on the Firewire physical device to confirm the proper operation of the interface.

10/100BASE-TX Ethernet Interface

This test confirms the proper operation of the ethernet interface. The core performs read and write cycles to registers on the ethernet physical device to confirm the proper operation of the interface. In addition, a collision test, as specified in the device datasheet, is completed. The operation of the status LEDs for the ethernet interface are manually verified through the selection of the technology input switch positions.

Table 68 lists error detection code is used to identify an interface that failed the test. LEDs `D[13..12]` are used to display this error detection code.

Table 68. Firewire Test Error Detection Codes

Interface	Error LED	Done LED
Firewire core	D12	D13
Ethernet core	N/A	N/A

Mix_Text_5

The Mix_Test_5 performs tests on the EPROM configuration device and FLASH interfaces.

EPROM Configuration Device Interface

This test confirms the proper operation of the EPROM configuration device memory. Several reads are performed which include not only 32-bit wide accesses, but also 16 bit read cycles to test the word lane control signals. The core first reads eight 32-bit values followed by eight 16-bit accesses to one word lane. Eight more 16-bit reads are performed to the other portion of the bus. In each case, the received data is compared to the expected value corresponding to the preprogrammed test pattern present in the EPROM device, signaling an error if they do not agree.

FLASH Interface

This test confirms the proper operation of the FLASH memory. Both reads and writes are performed including not only 32-bit accesses, but also 8-bit cycles to test the byte lane control signals. In addition, the address convergence testing of the general purpose memory bus is performed using the Flash memory. The core first erases the entire Flash memory. The address convergence test is then performed, using 32-bit accesses, writing a unique value to all addresses and reading each memory location to ensure the presence of the correct data. A portion of the memory is erased to allow four 8-bit write cycles to be completed, testing the byte lanes control signals. A single 32-bit read is performed to verify these byte-sized writes.

The following error detection code is used to identify an interface that failed the test. LEDs `D[14..11]` are used to display this error detection code.

Table 69. FLASH & EPROM Test Error Detection Codes

Interface Core	Error LED	Done LED
Flash core	LED11	LED13
EPROM core	LED12	LED14

SDRAM_top

This test confirms the proper operation of the SDRAM memory operating at 66 MHz. Both reads and writes are performed including not only 32-bit accesses, but also 8-bit cycles to test the byte lane control signals and both burst read and write accesses. In addition, the data convergence testing of the general-purpose memory bus is performed using the SDRAM memory. The core first initializes the SDRAM, then performs the walking one's and zero's data convergence test on the data bus. Eight individual 8-bit writes are performed followed by two 32-bit reads to verify the data to confirm the byte lane control signals. Finally, the core performs a burst write of length four followed by a burst read of length four. A pass is communicated by the illumination of LED D13. A failure is communicated by the illumination of LED D11.

LCD_top

The LCD_top core is downloaded onto the EPC2 devices. When the board is powered up, and the LCD_top core is programmed in the EPC2s, the LCD interface displays the phrase "SOPC Development Board" indicating that the LCD interface is functioning correctly.

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