



Optimizing Performance using 65-nm Architecture

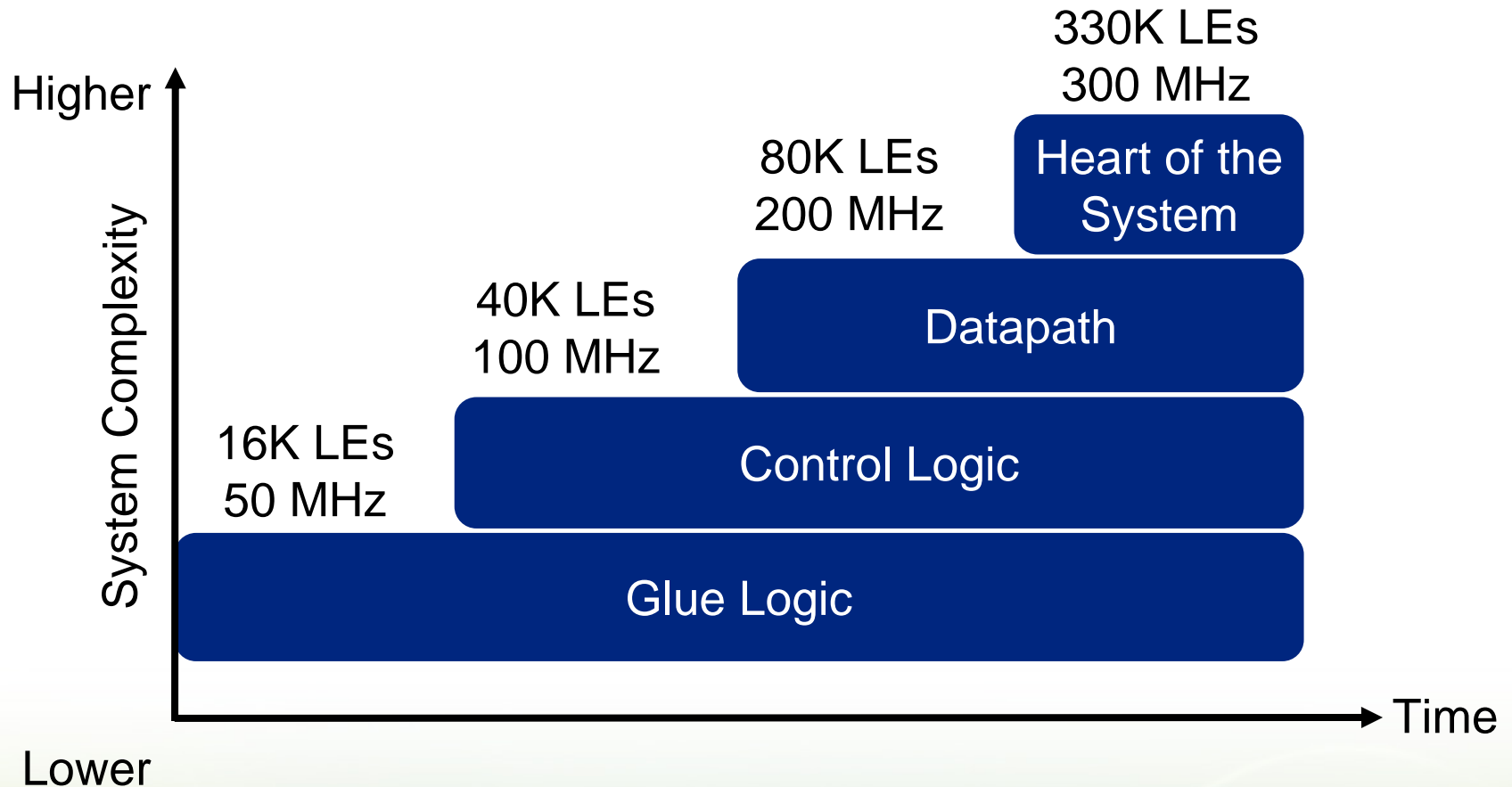
Agenda

- Evolution of FPGAs and customer challenges
- Stratix[®] III architecture designed for high performance
- Performance benchmarks for Stratix III FPGAs
- Power optimization in Stratix III FPGAs
- Summary



Evolution of FPGAs—Usage and Customer Challenges

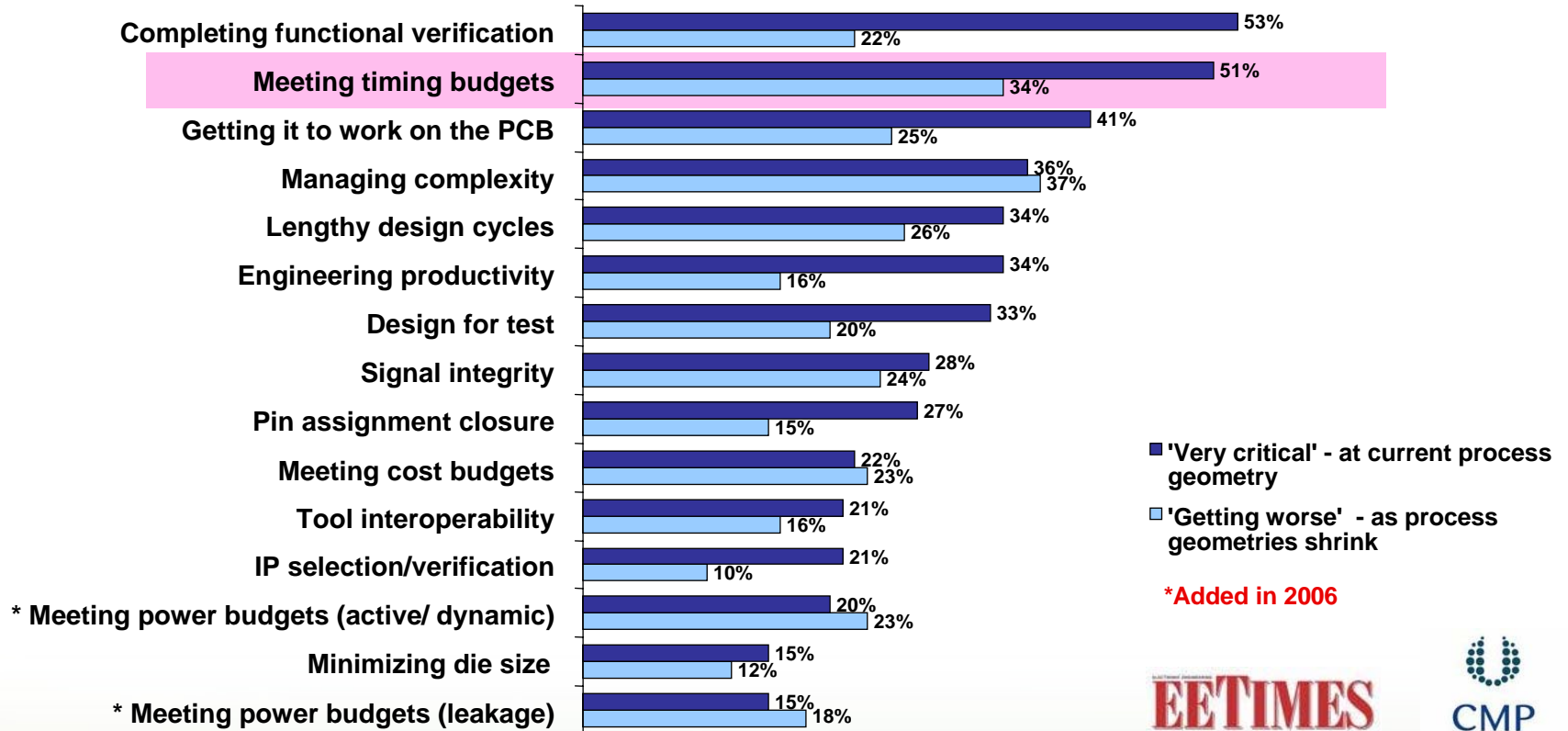
Evolution of FPGA Usage



Today's FPGAs Have Evolved

Issues and Challenges in FPGA Projects for Asia

EETimes - 2006 EDA Times Study



EETIMES



Performance, Productivity, Power, and Price



Stratix III FPGAs Address FPGA Design Challenges



■ Performance

- Industry's highest performance FPGA

■ Power

- Industry's lowest power high-end FPGA with innovative Programmable Power Technology



- Net Seminar: *Learn to Design with Stratix III FPGA's Programmable Power Technology and Selectable Core Voltage* (April 2007)



QUARTUS® II

■ Productivity

- Quartus® II software: #1 in performance and productivity
- Net Seminar: *How to Maximize Performance and Productivity for Stratix III Using Quartus II Software* (June 2007)



■ Price

- Patented redundancy reduces cost automatically
- Risk-free path to structured ASIC – HardCopy® devices
- Please visit www.altera.com for more details



Benefits of Higher Performance

- Allows faster time-to-market
 - Reduces effort for timing closure
- Provides extra operating margins for extreme conditions
- Saves cost
 - Achieves performance goals with lower speed grade devices
 - Serializes parallel logic to use lower density device
- Allows path for future system upgrades
- Provides extra horsepower if your design needs it



Achieving Performance using Stratix III Devices

Stratix III FPGAs Built with Performance in Mind

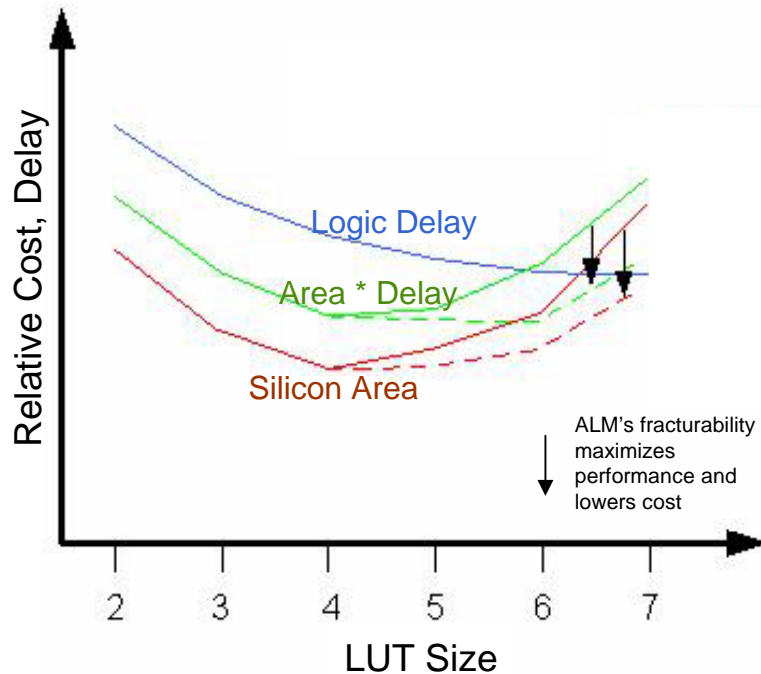
- Advanced 65-nm process
- High-performance architecture
- Integrated tools solution with Quartus II software

Stratix III FPGAs Built on Leading-Edge Process Technology

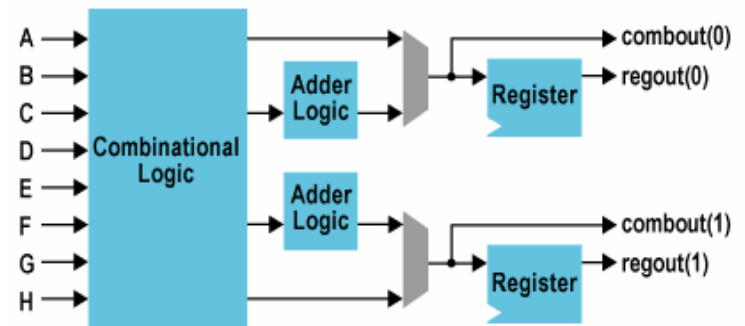
- Advanced 65-nm process
 - 15% capacitance reduction → reduces dynamic power and increases performance
- Strained silicon
 - Increased performance
- Low-k inter-metal dielectric
 - Reduces dynamic power, increases performance
- Copper interconnect
 - Increased performance, reduced IR drop
- Multiple-gate oxide thicknesses (triple oxide)
 - Trade-off of power vs. speed per transistor
- Multiple-threshold voltages
 - Trade-off of power vs. speed per transistor

Stratix III FPGAs Built for Increased Performance and Reduced Power

Innovative Adaptive Logic Module

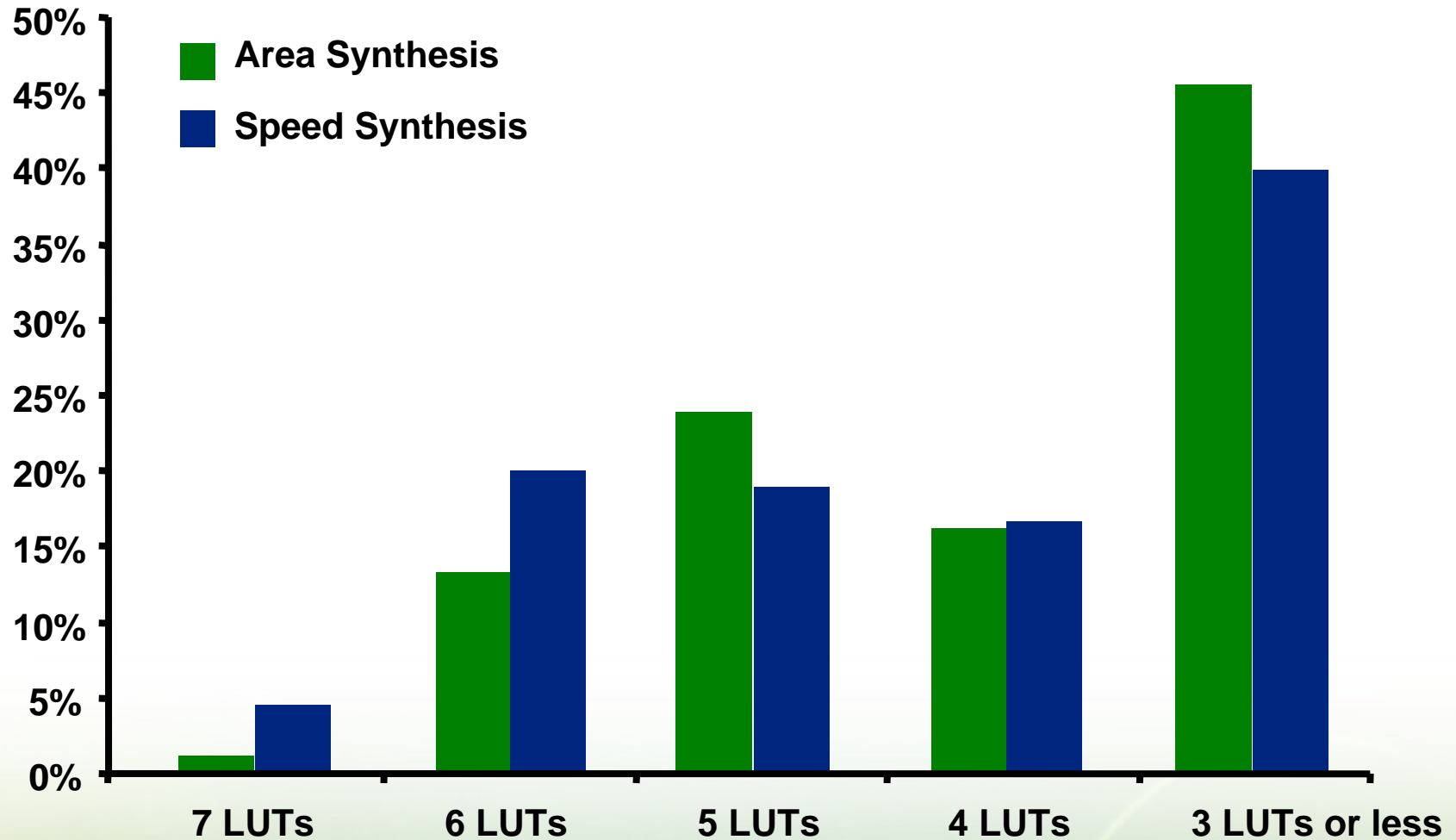


Innovative adaptive logic module (ALM) introduced in 2004



Stratix III FPGAs Built On a Highly Flexible ALM Architecture

One Look-up Table (LUT) Size Does Not Fit All



* Results on real customer benchmarks

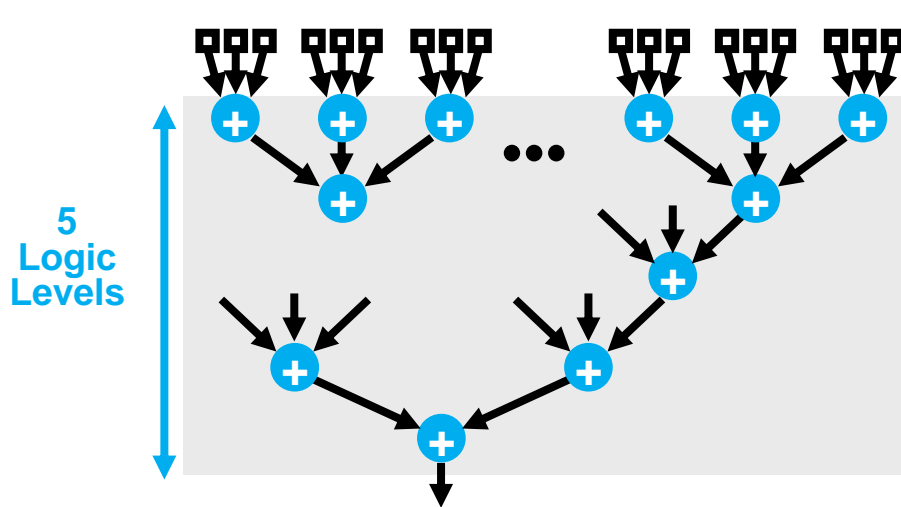
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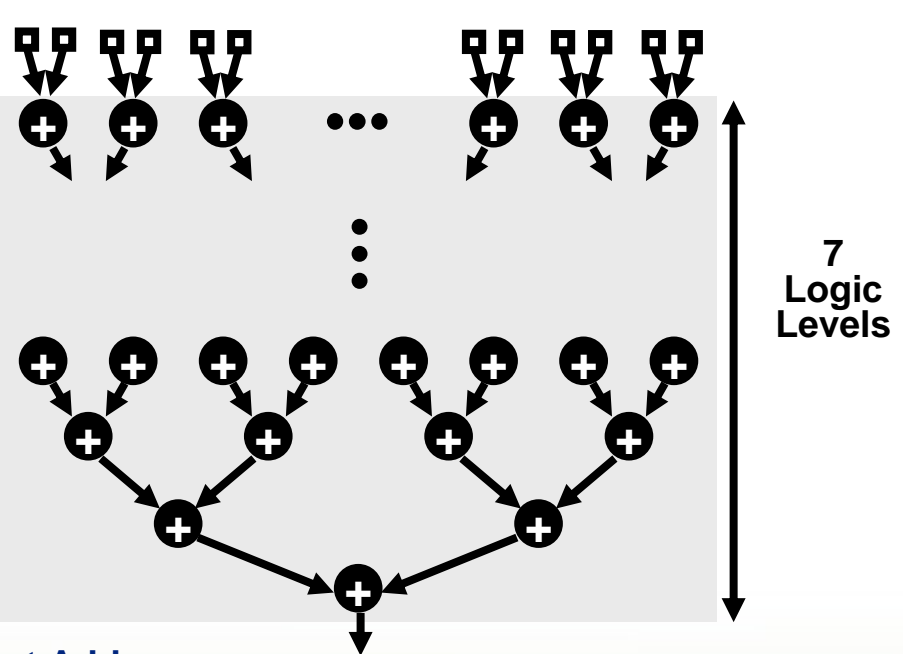


ALM Adder Tree Support

Stratix III ALM 3-Input Adder Tree



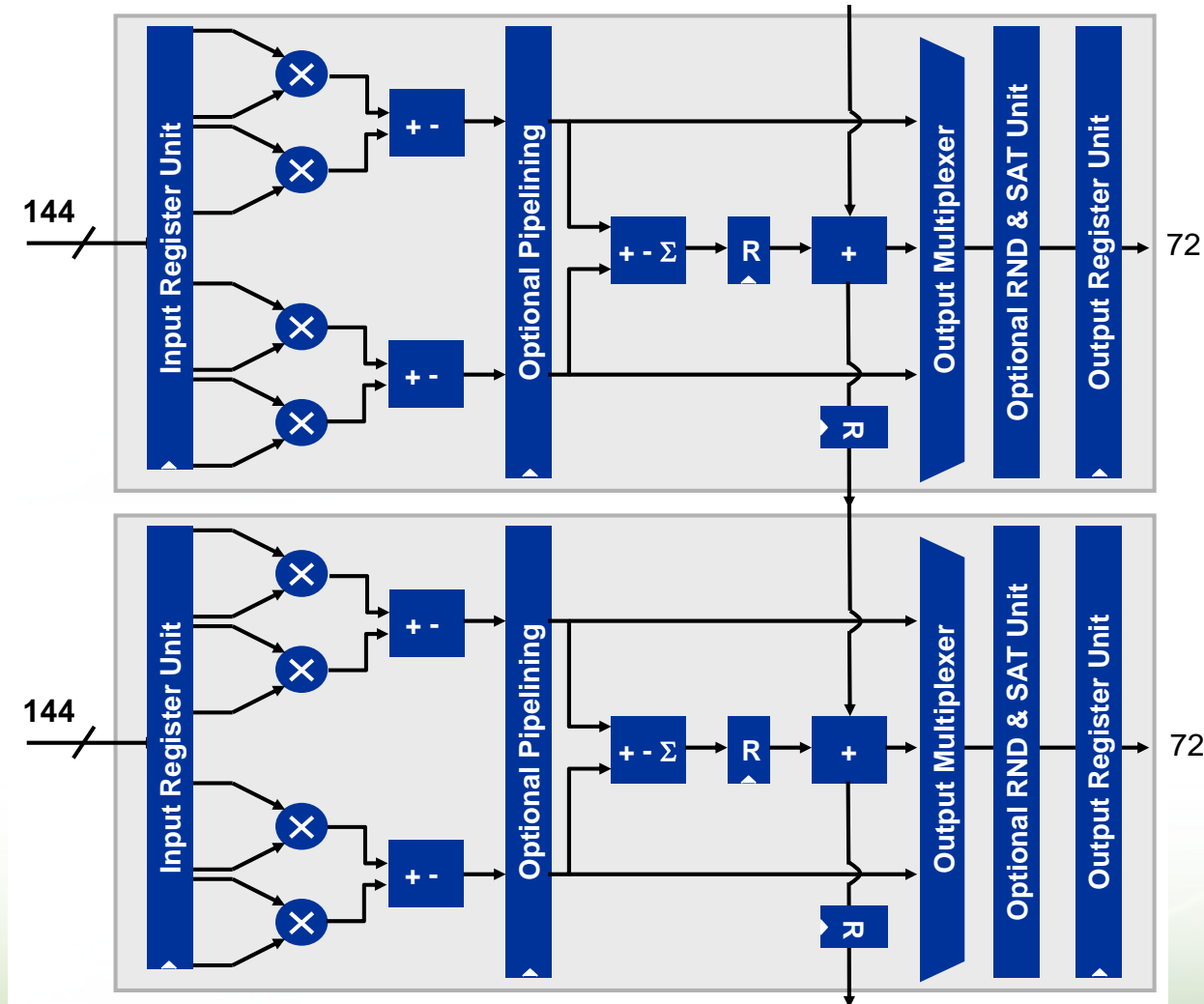
2-Input Adder Tree



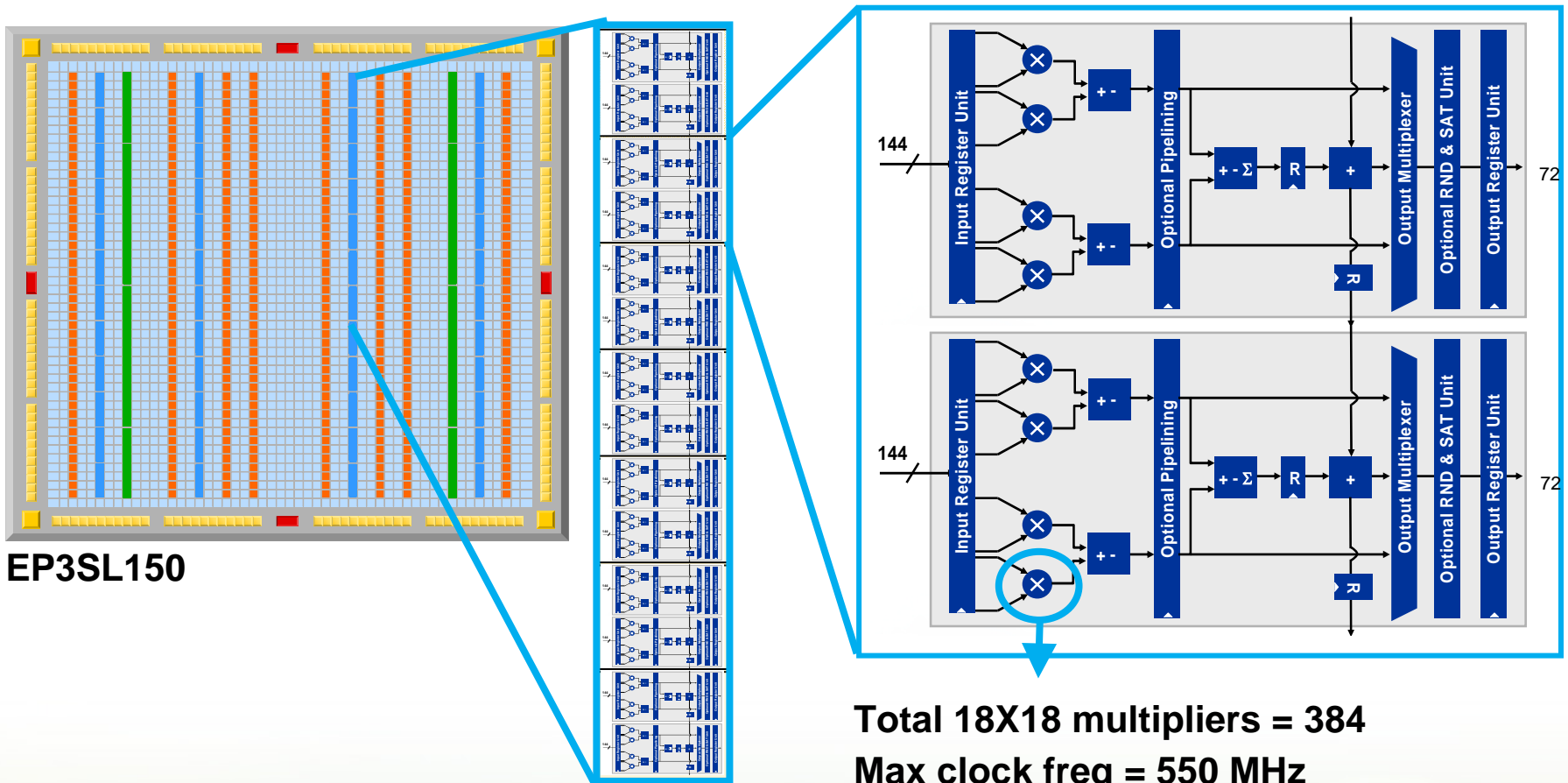
16-Bit 128-Input Adder

Less Logic Required – Increased Performance

Stratix III DSP Block Summary



Performance Through Parallelism



Total 18X18 multipliers = 384

Max clock freq = 550 MHz

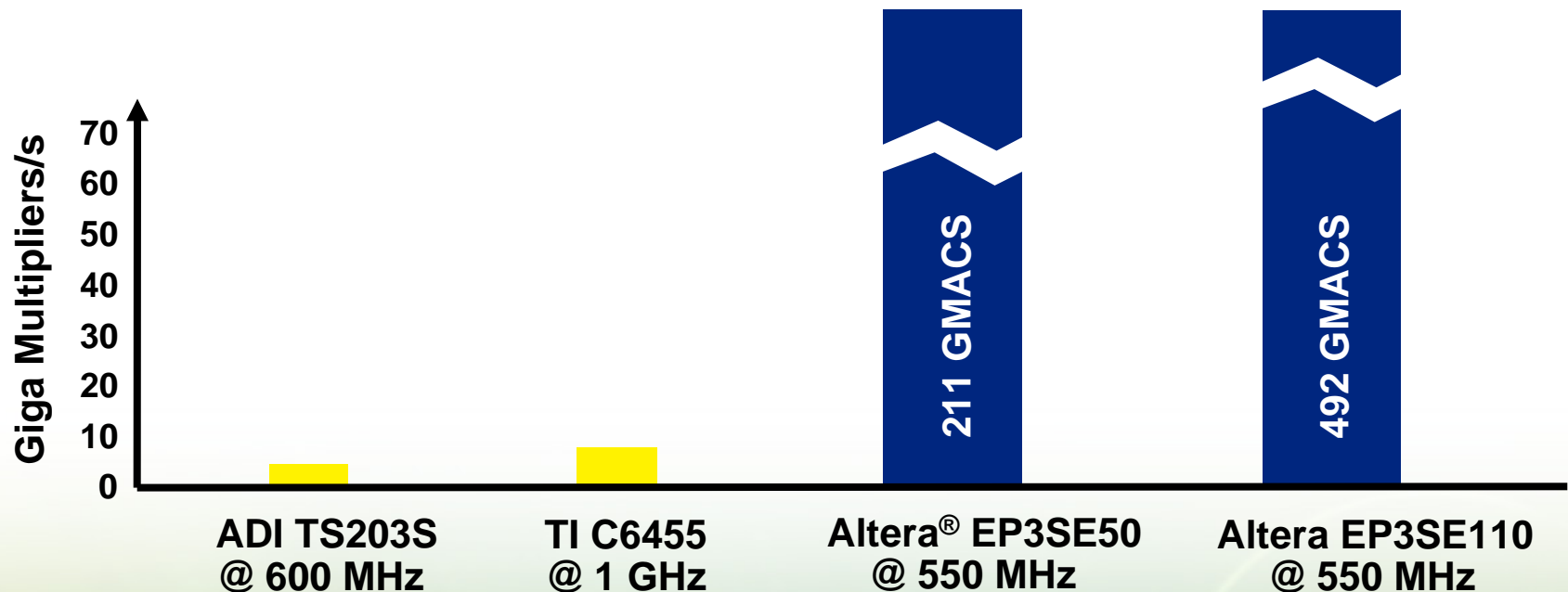
Max performance = 384 * 550 MHz

211 GMACS



DSP Advantages of Stratix III FPGAs

- Stratix III FPGAs deliver 50X performance over dedicated digital signal processing (DSP) devices
 - Parallel processing
 - High memory- and multiplier-to-logic ratios



Stratix FPGAs for High-Performance DSP



Stratix III EP3SL70* @
300 MHz
86 GMACS
~3 Watts
~1,225 mm²
~\$400 in 1KU

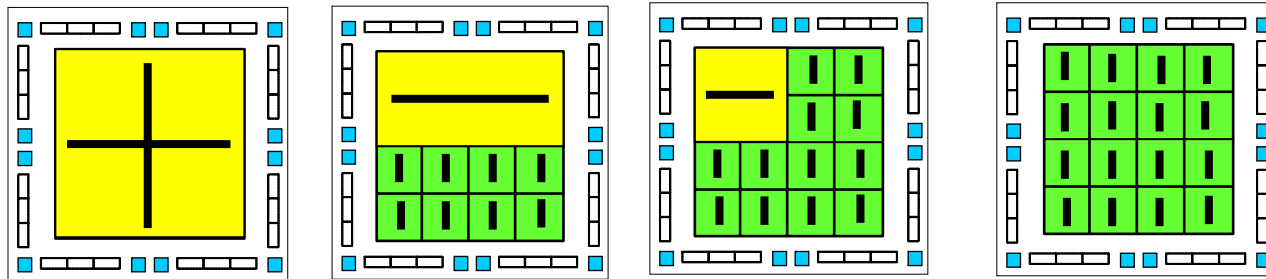
*Note: Stratix III EP3SL70
FPGA is small logic-oriented
device

*For Equivalent Performance, Stratix III FPGAs Provide
Lower Cost, Low Power, and Reduced Board Space*

Clock Networks and PLLs

■ Abundant clock resources

- Easy placement and routing utilizing a 600-MHz clock network
- Up to 88 regional clock networks for fewer fanouts and fast local clock



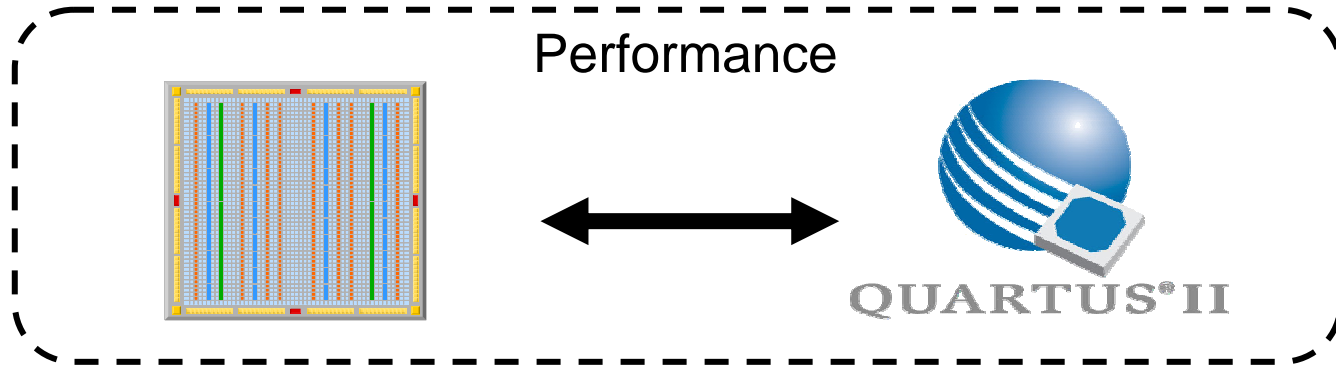
All clock networks automatically powered down when not in use

■ High-performance and flexible phase locked loops (PLLs)

- Up to 12 PLLs per device, each with up to 10 outputs per PLL
- 5- to 720-MHz output with inherent jitter filtration

High-Performance Clocking Scheme at 600 MHz

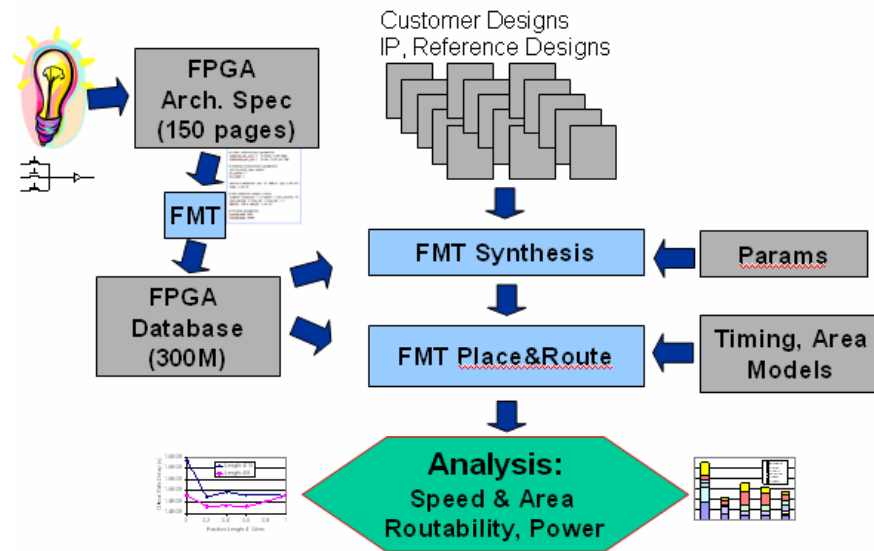
Software-Driven Architecture



- Architecture-optimized software tool implementation critical to achieve
 - Increased performance and reduced power
 - Efficient logic utilization
 - Enhanced productivity

FPGA Architecture Only as Good as the Software Can Exploit

Quartus II Software Fully Optimized for Stratix III FPGAs



■ Altera's FPGA modeling tool (FMT)

- Enables Altera to virtually model a variety of FPGA structures to achieve an optimal, well integrated architecture
- FMT provides in-depth modeling capabilities and their effects on performance, area, and cost

Quartus II Key Features

- Design space explorer
 - Automated utility to find settings for the best performance
- Incremental compile
 - Optimizes performance by block and maintains the overall performance
- TimeQuest timing analyzer
 - Supports Synopsys Design Constraint (SDC), an industry-standard tool, for faster analysis of advanced design constructs
- PowerPlay optimization
 - Localizes high-toggling nets, and routes for minimum capacitance to maximize your performance while lowering power

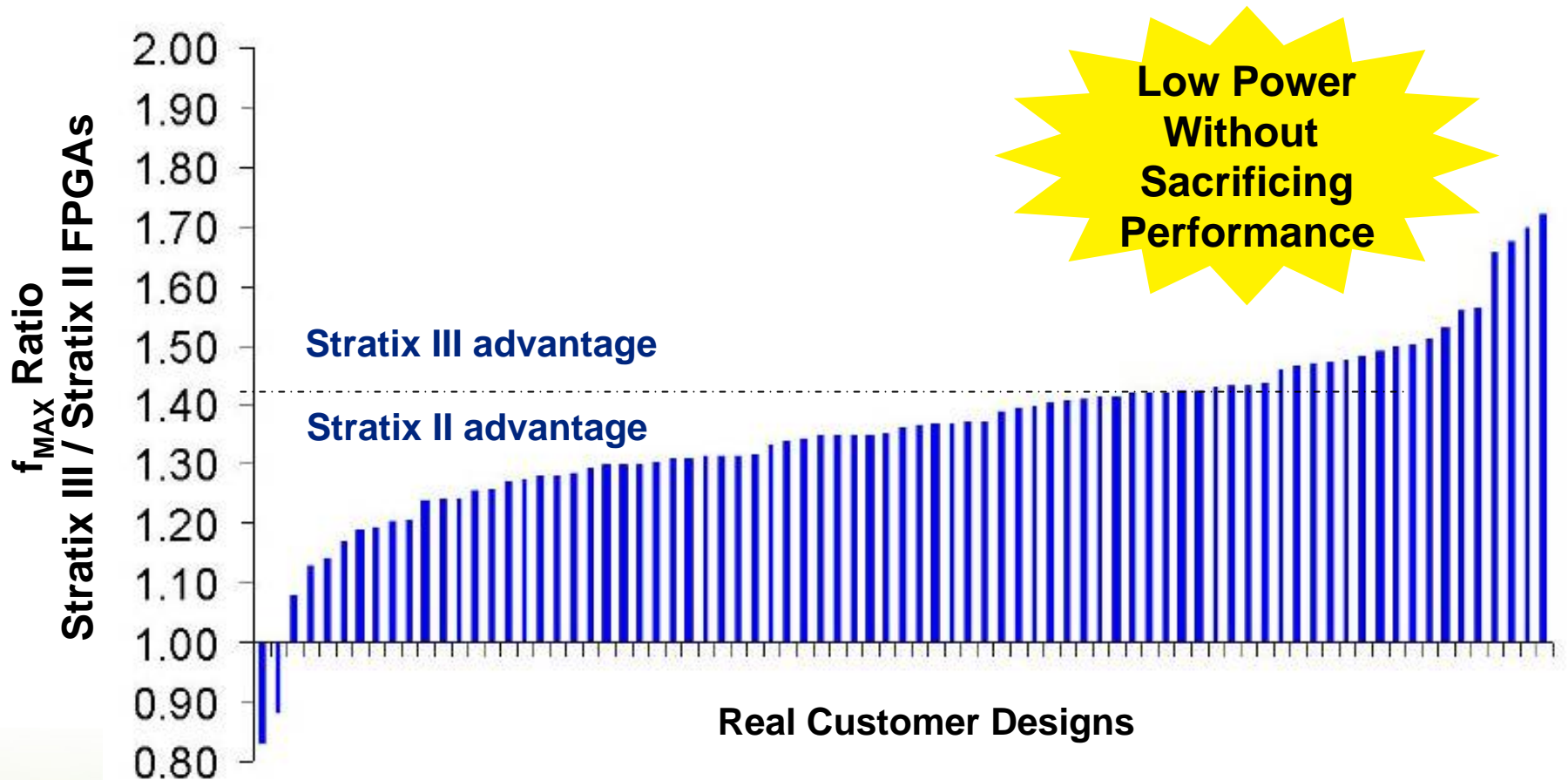
Quartus II Software is Stratix III FPGA--Ready





Performance Comparison of Stratix III and Stratix II FPGAs

Stratix III FPGAs: Highest Performance



Stratix III FPGAs are 35% Faster than Stratix II FPGAs

Stratix III FPGA Performance Scorecard

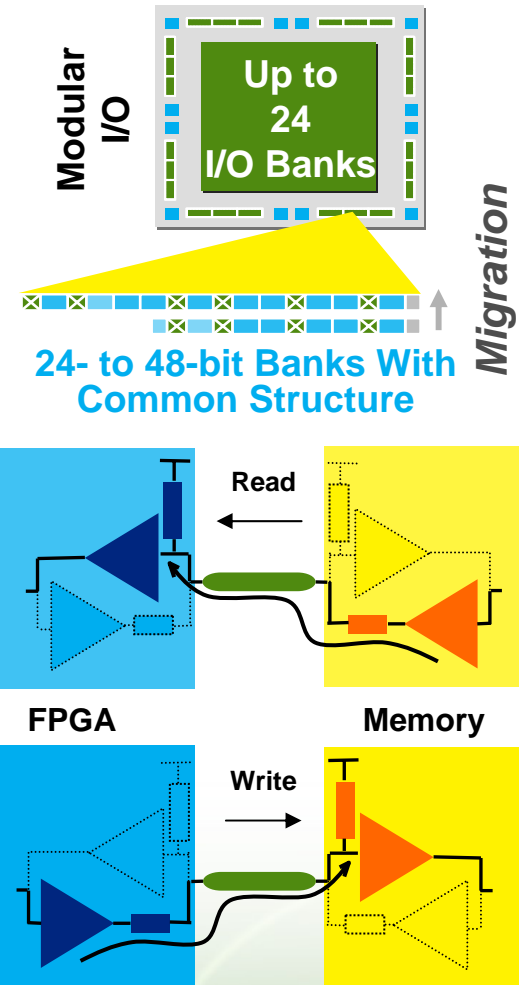
Block	Stratix II Devices	Stratix III Devices **
Logic Fabric	500 MHz	600 MHz
Small RAM	500 MHz	600 MHz
Medium RAM	550 MHz	600 MHz
Large RAM	400 MHz	600 MHz
DSP Block	450 MHz	550 MHz

** Pending characterization

Stratix III FPGA I/O Connectivity



- High flexibility and efficiency
 - Modular bank structure
 - Supports over 40 industry I/O standards with adjustable slew rate, drive strength, and output delay
 - Dynamic trace compensation for trace mismatch per I/O
- Enhanced on-chip termination (OCT)
 - Dynamic OCT changes termination dynamically
 - Calibration gives repeatable and predictable termination

High-Performance I/Os



I/O Performance

- LVDS and external memory interfaces support on all I/O banks

Interconnect	Device Family	
	Stratix II FPGA Definition	Stratix III FPGA
	Performance	Performance * **
DDR3 	N/A	400 MHz
DDR2	333 MHz	400 MHz
QDR II	300 MHz	350 MHz
QDR II+ 	N/A	350 MHz
RLDRAM II	300 MHz	400 MHz
LVDS	1.0 Gbps	1.25 Gbps
	Dynamic Phase Alignment (DPA)	Dynamic Phase Alignment (DPA)
PCI, PCI-X	3.3-V Compliant	3.3-V Compatible

* Stratix III FPGA left and right banks support 300-MHz DDR.

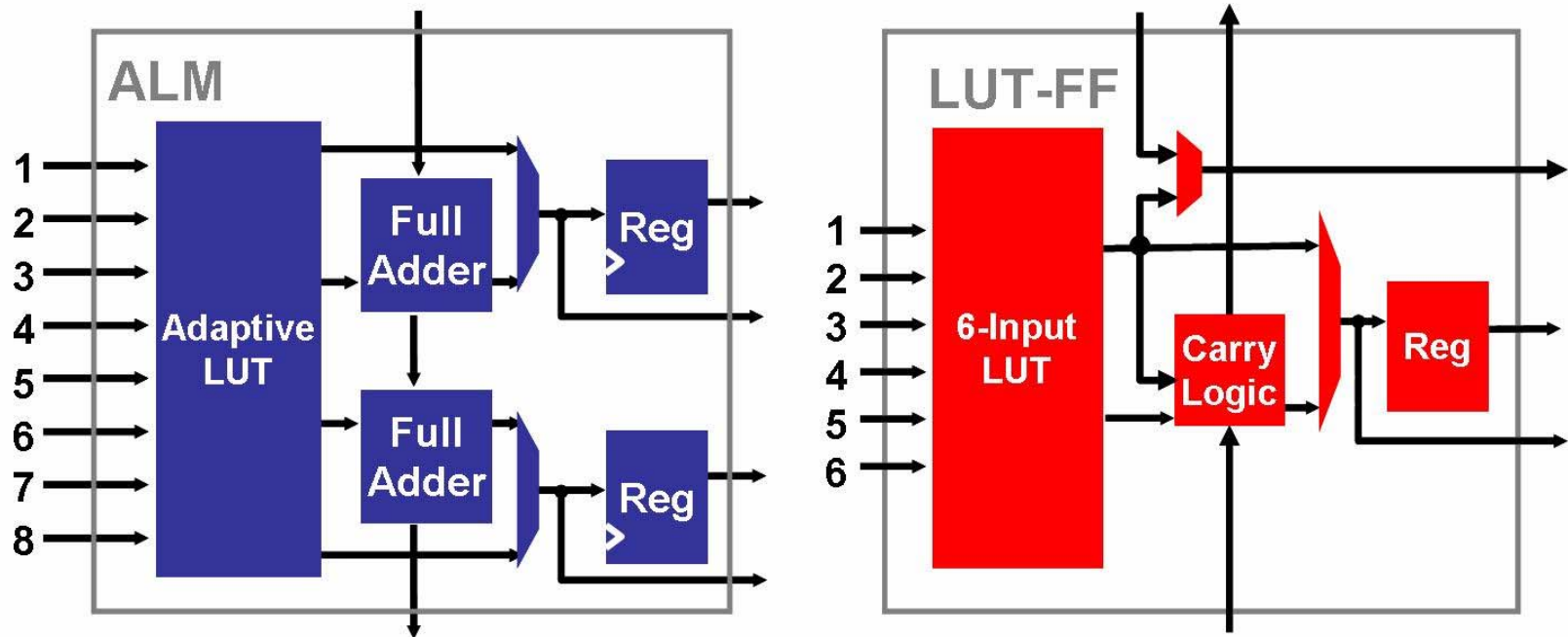
Stratix III FPGA top and bottom banks support 800-Mbps LVDS input and 500-Mbps output using a 3-resistor network.

**Pending characterization



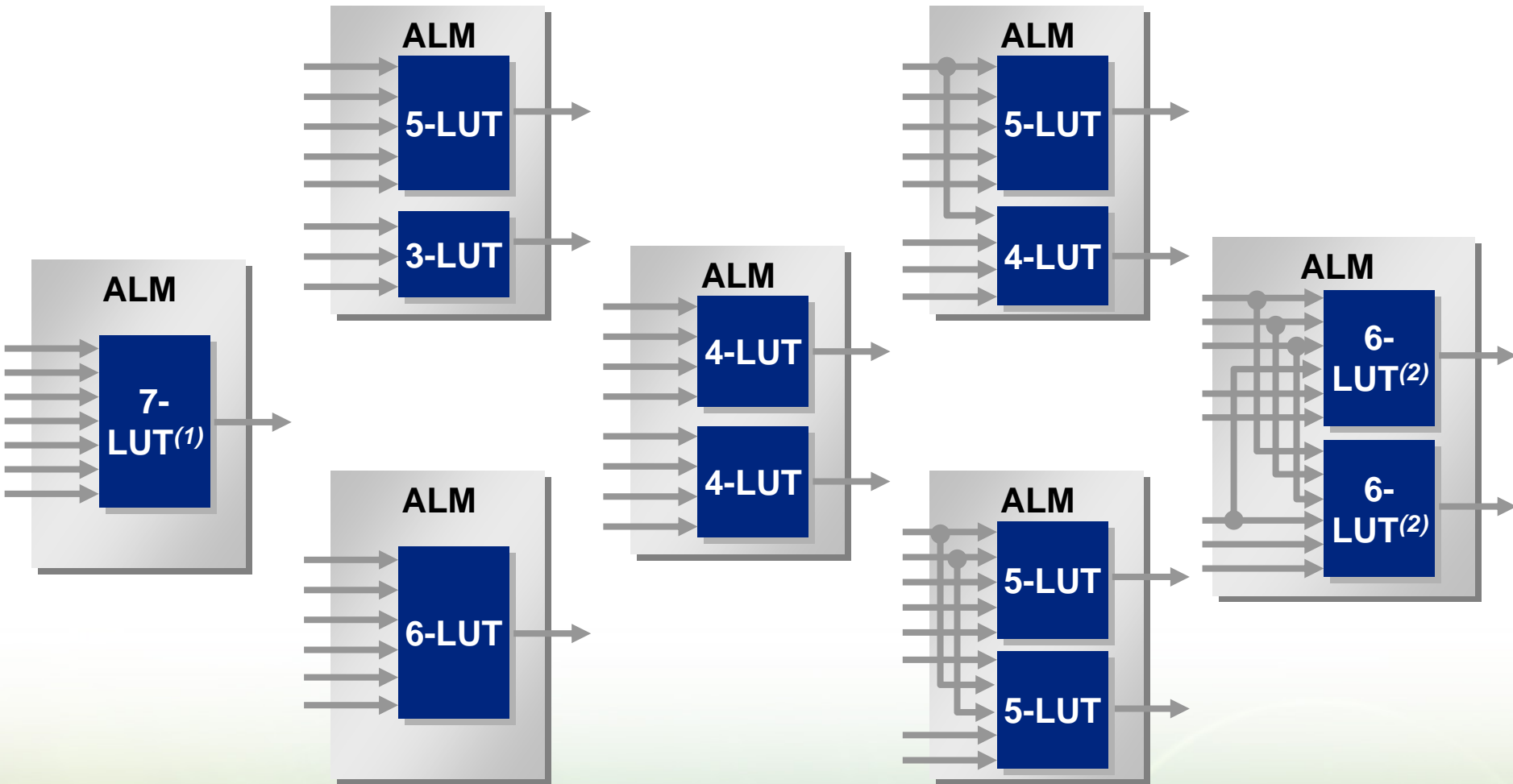
Architecture Comparison of Stratix III and Virtex-5 FPGAs

Stratix III ALM vs. Virtex-5 LUT-FF Pair



Stratix III ALM—Flexible, Efficient, and Industry's Best FPGA Logic Architecture

Stratix II ALM 8-Input Fracturable Architecture



(1) Stratix II ALM can implement a subset of 7-input functions

(2) Must have same logical function

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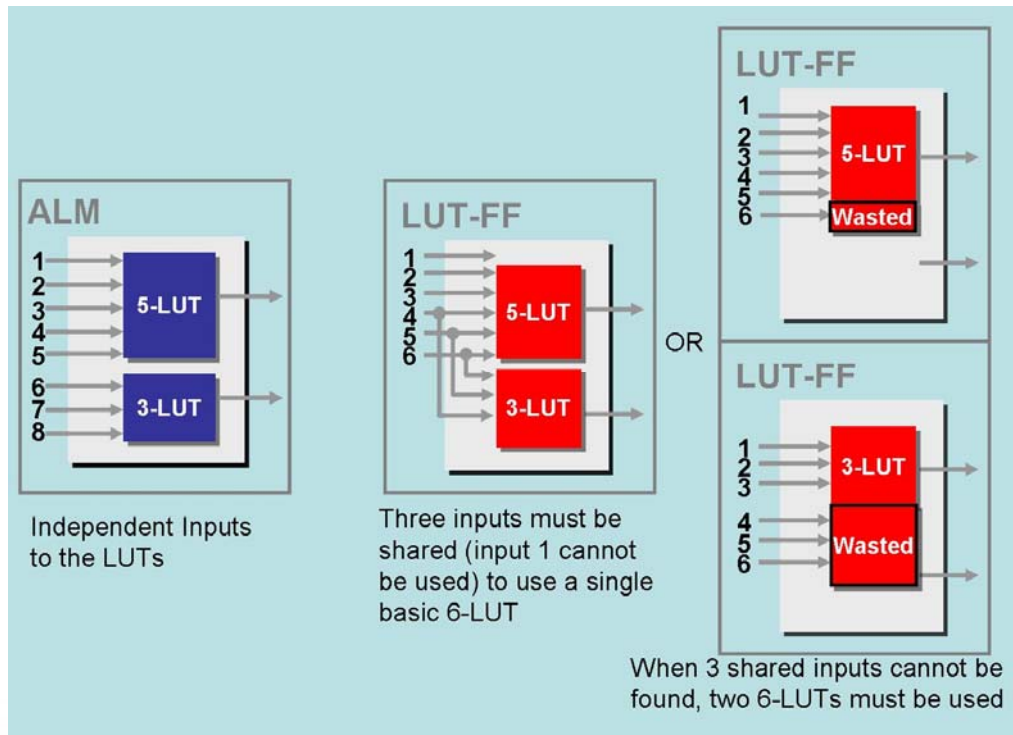
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LUT Mapping to 6-LUT and ALM

Output 1	Output 2	V-5 minimum # shared inputs	ALM minimum # shared inputs
5-LUT	5-LUT	5	2
5-LUT	4-LUT	4	1
5-LUT	3-LUT	3	0
4-LUT	4-LUT	3	0
4-LUT	3-LUT	2	0
3-LUT	3-LUT	1	0



Stratix III 8-Input Fracturable LUT vs. Virtex-5 LUT- FF Pair

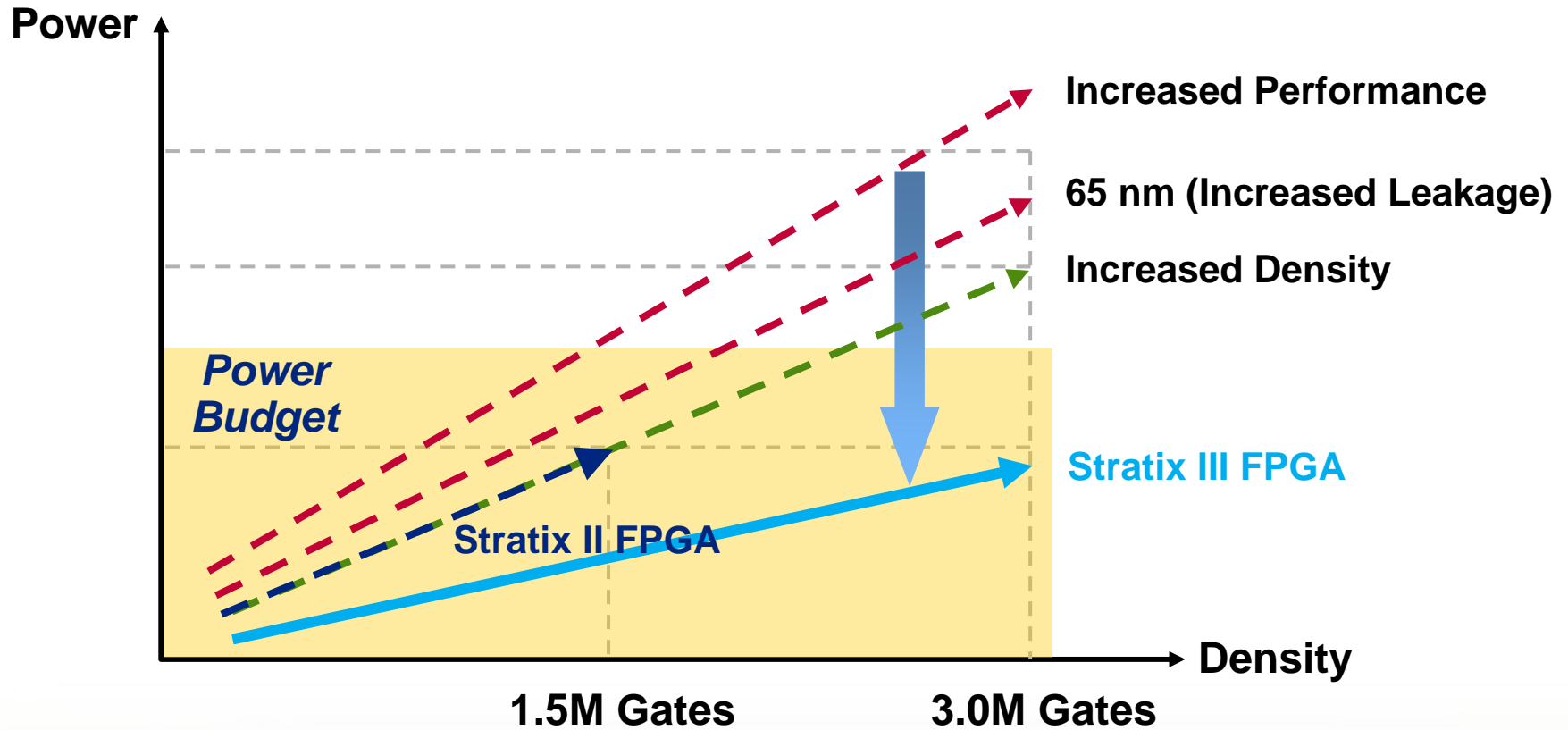


*ALM Packs More Logic Efficiently
for Higher Performance*



Optimizing Power in Stratix III FPGAs

Meeting the Power Challenge



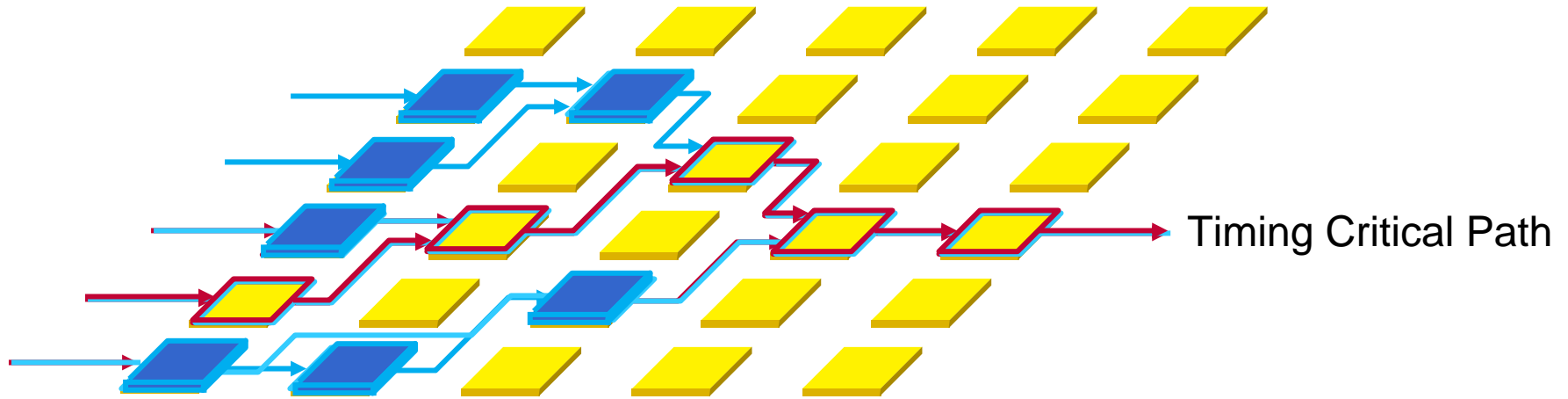
*Stratix III FPGAs Cut Power
by 50% vs. 90 nm*

Lowest Power FPGA in the Industry

Stratix III FPGA Power Reduction Technique	Lower Static Power	Lower Dynamic Power
Silicon Process Optimizations	✓	✓
Selectable Core Voltage (0.9 V or 1.1 V)	✓	✓
Programmable Power Technology	✓	✓
Power-Optimized DDR Memory Interface	✓	✓
Quartus II Software PowerPlay Power Analysis and Optimization	✓	✓

Programmable Power Technology

Logic Array



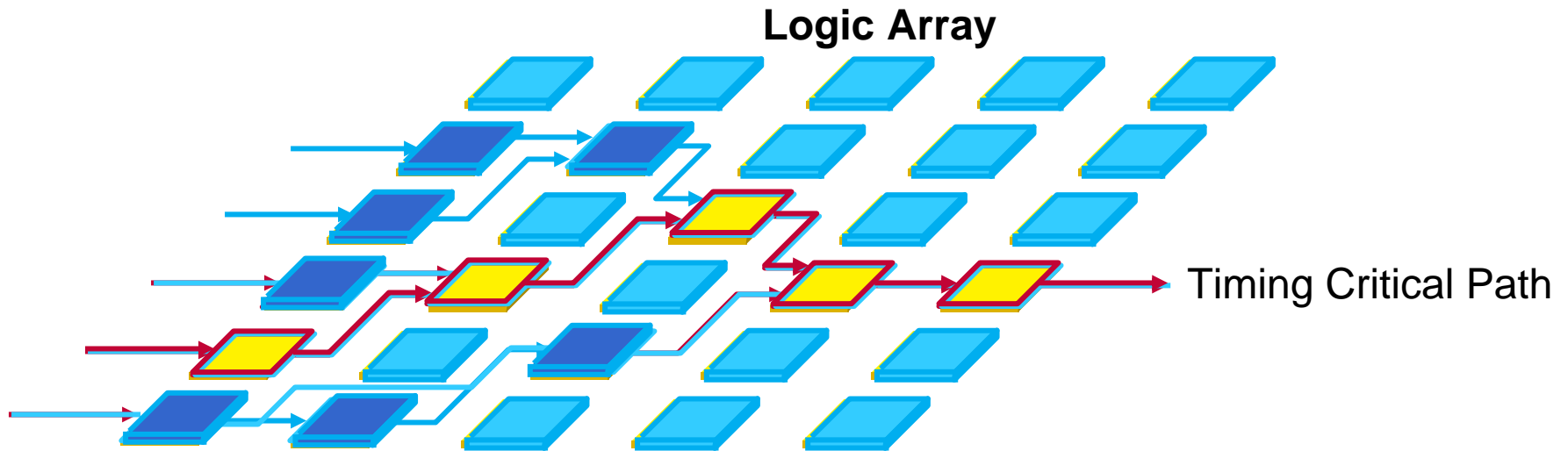
High-Speed Logic



Low-Power Logic



Programmable Power Technology



* Power mapping fully automated by Quartus II software based on timing constraints

High-Speed Logic



Low-Power Logic



Unused Low-Power Logic



*High Performance Where You Need It,
Lowest Power Everywhere Else*

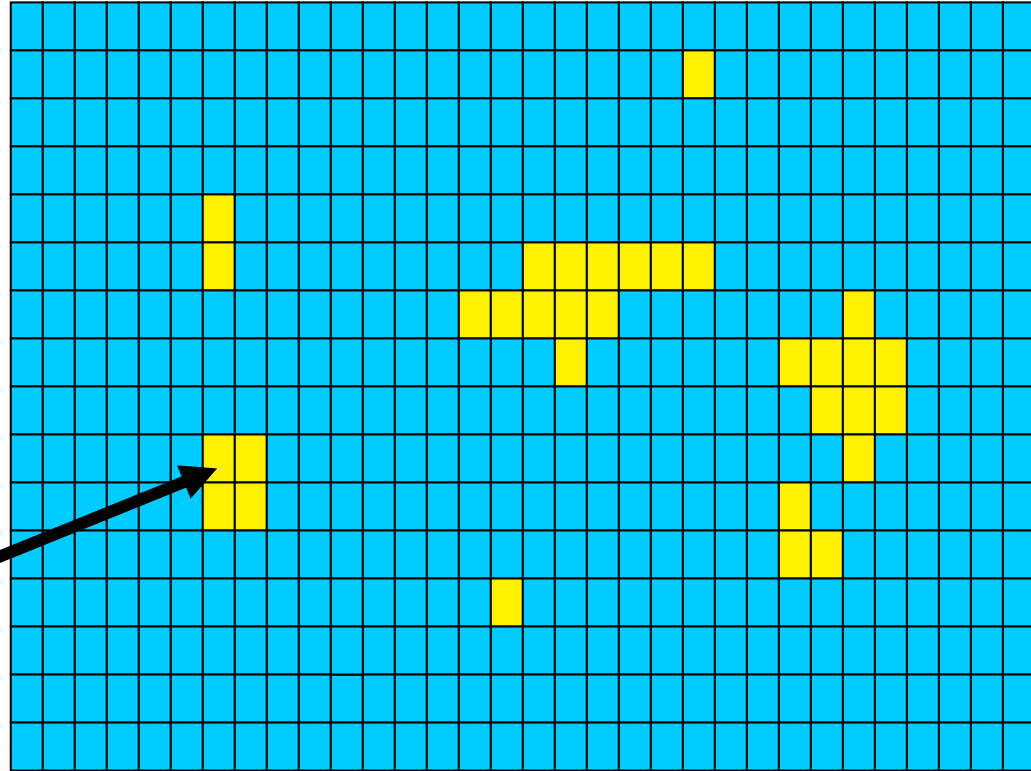
High Speed/Low Power

- Low-power mode for a tile results in
 - 60% reduction in static power
 - 5% reduction in dynamic power
 - ~20% increase in delay
 - Quartus II CAD system doesn't use low-power mode on critical paths
 - No impact on system speed
- Tiles can be
 - Pair of logic array blocks (LABs)
 - RAM block
 - DSP block

High-Resolution Power Control

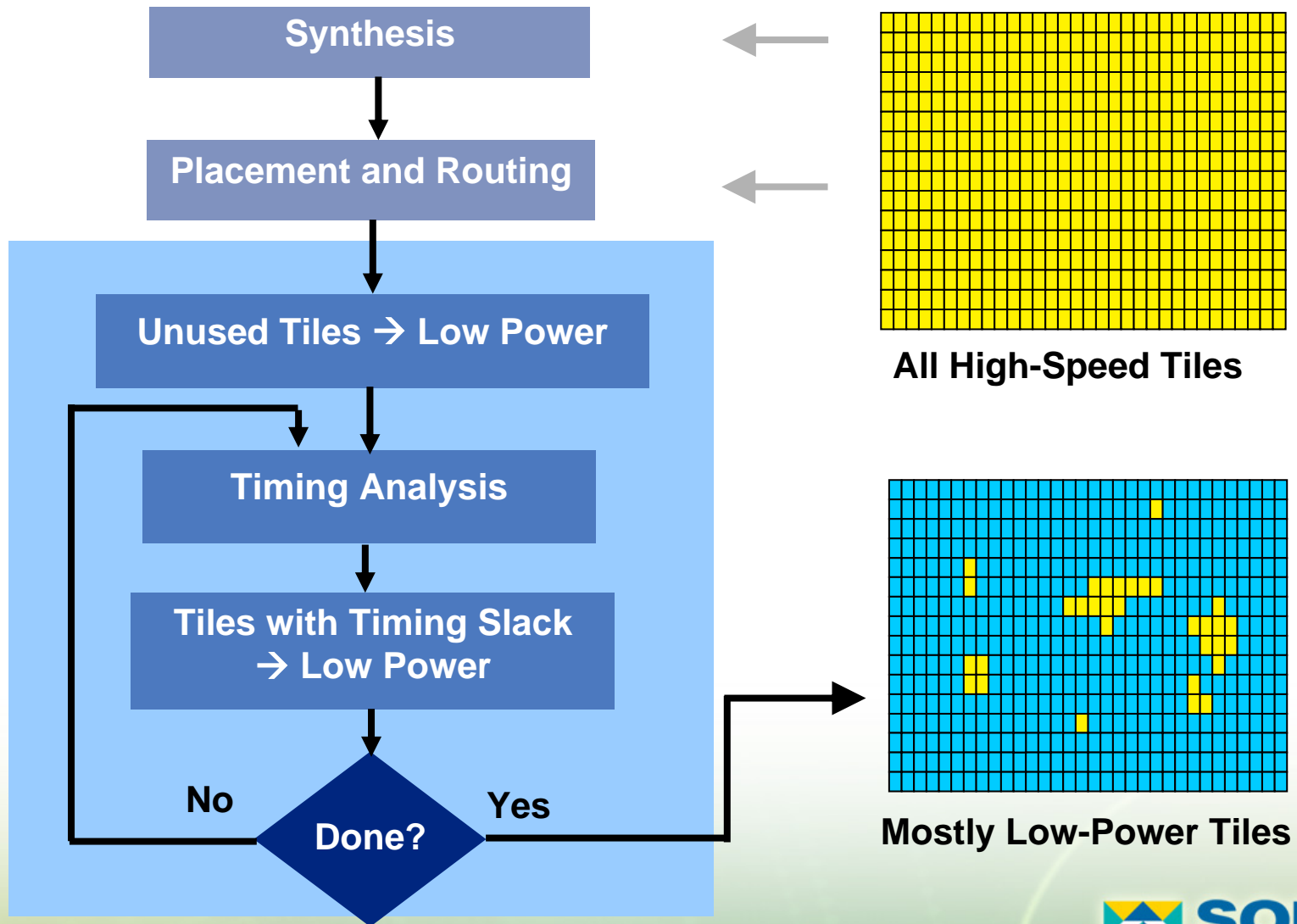
Stratix III FPGA
(EP3SL340) has **8,050**
tiles for very high-
resolution
power/performance
optimization

Only a small
percentage of high-
speed tiles required
to maintain design
performance

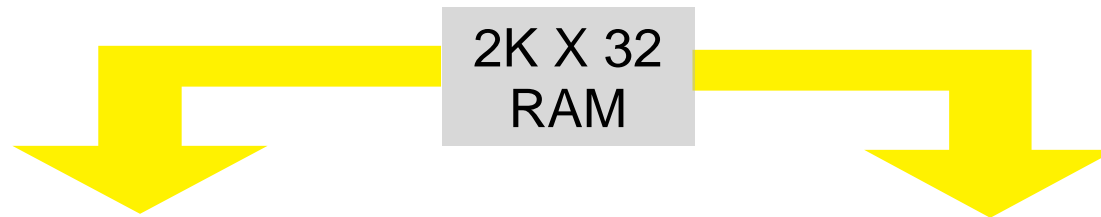


*Speed of the Fastest LABs,
Power of the Slowest*

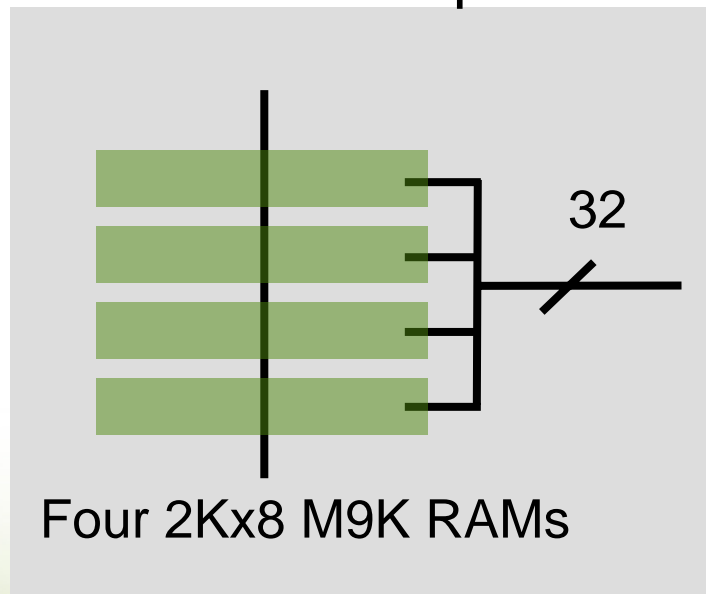
Automatic Programmable Power



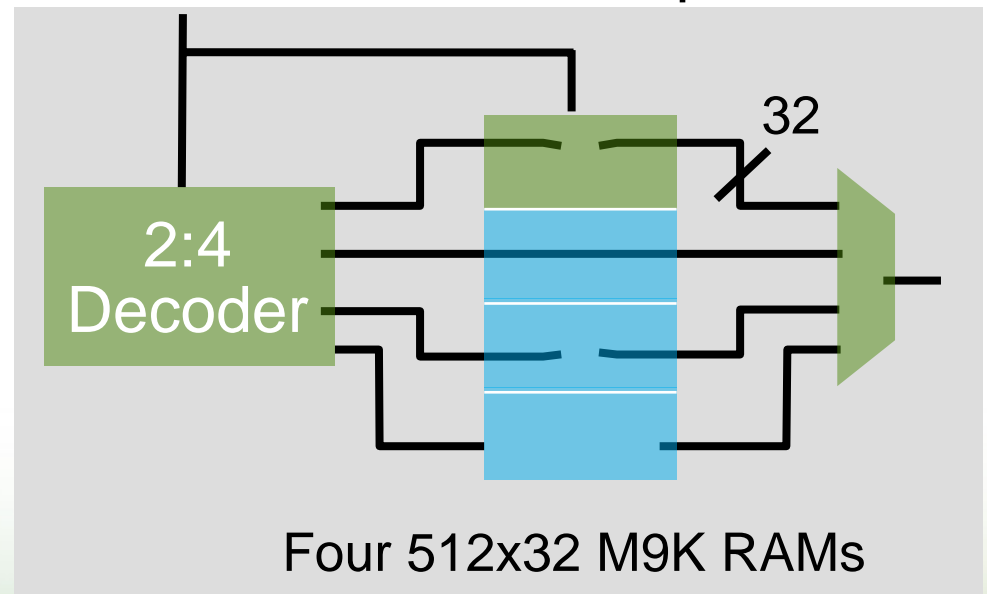
Example: Power-Optimized RAM Mapping



Default Option



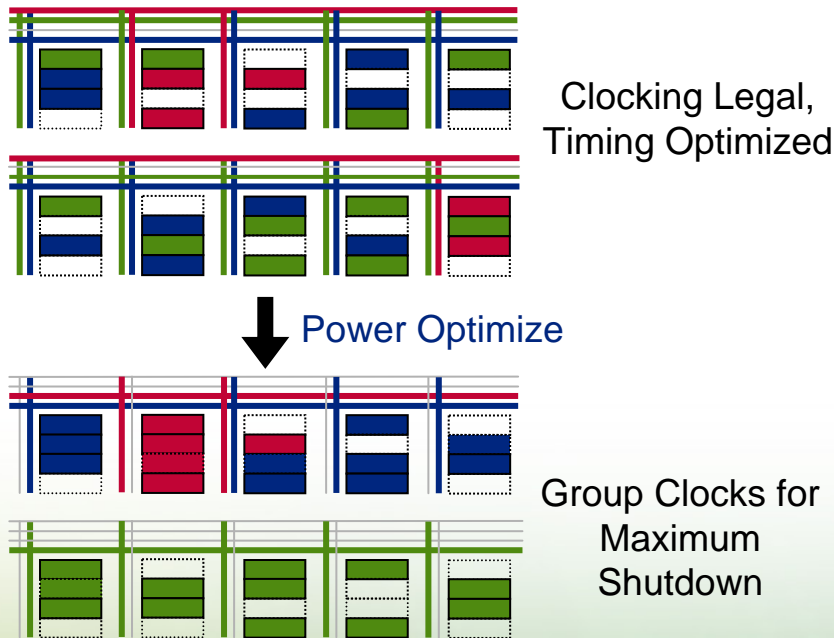
Power-Efficient Option



Logic and Clock Power Optimization

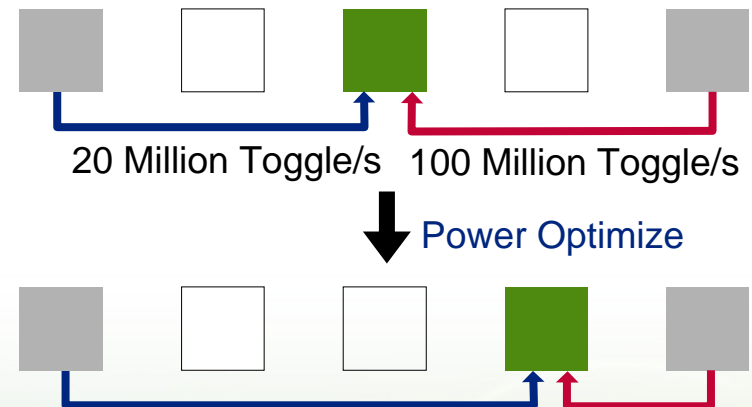
■ Clock power reduction

- Stratix III hardware can shut down clock at 3 levels of tree
- Automatic placement to reduce clock power

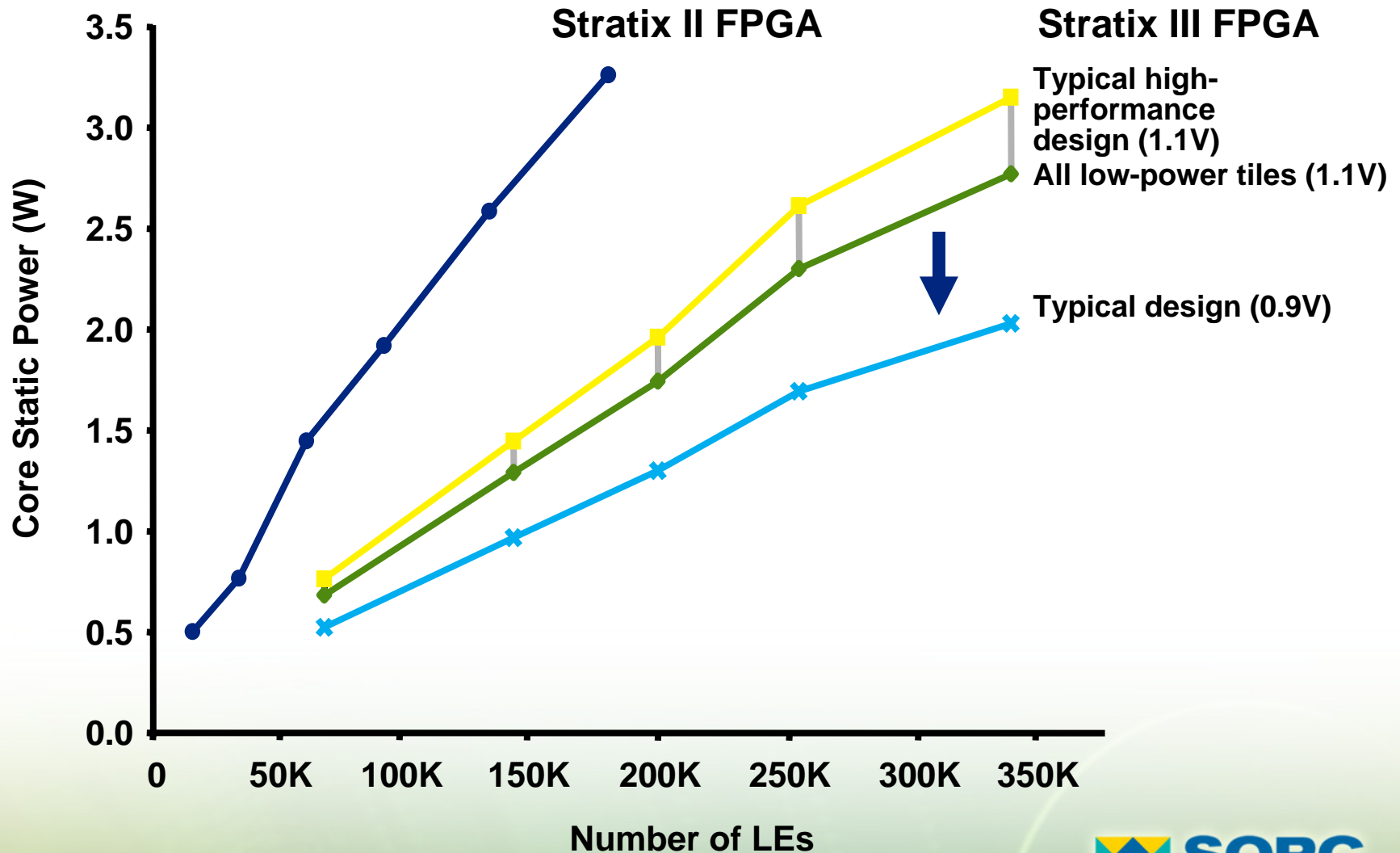


■ Power-driven placement and routing

- Minimize capacitance of high-toggling signals
- Without violating timing constraints

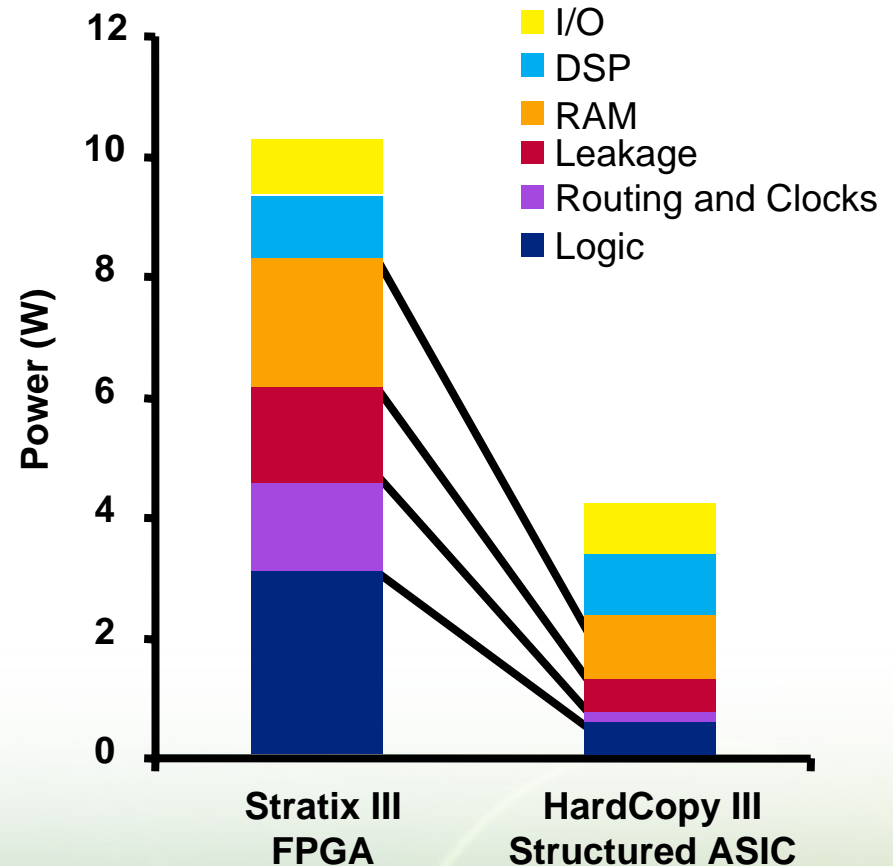


60% Lower Static Power (85° C)



HardCopy III Structured ASICs - Designed for Low Power

- Structured ASIC – optimized architecture for power efficiency
- Unused logic and memory blocks not connected to power rail
- Unused clock trees and PLLs not powered
- Estimated power reduction from Stratix III FPGAs
 - >275 MHz: Up to 70%
 - >50 MHz and < 275 MHz: 30% to 70%
 - <50 MHz: Up to 30%



Summary

- Stratix III devices are the fastest FPGAs
 - Only FPGAs with a 600-MHz core clock speed
 - Supports high-speed DDR3 standard
- Stratix III FPGAs are, on average, one speed grade faster than Virtex-5 FPGAs



Thank You!