9 Registers

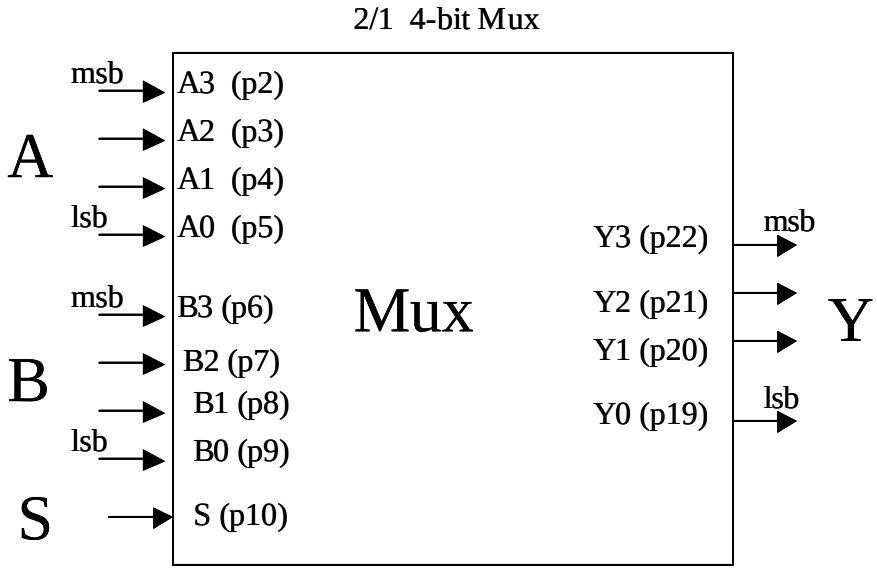
In a digital system it often necessary to work with several bits of data grouped together such as nibbles (4-bits), bytes (8-bits), etc. A basic component of such systems is the *m*-bit register. An *m-bit* register consist of *m* edge-triggered flip-flops with a common clock. A register has a control line called "load" that is used to load the register with a new value from an external bus. Registers can also have incrementing and shifting capabilities. In this experiment you will construct a 4 bit register. Note: This lab has Altera Maxplus requirements - see the prelab for details.

I. Devices Needed

You will need two 74LS74 ICs, a PLD programmed as a 2/1 4-bit mux,.and perhaps some 74XX gates for glue logic. The TA will program one of your PLDs as a 2/1 4-bit Mux. The mux implements the function: Y = A S + B S'

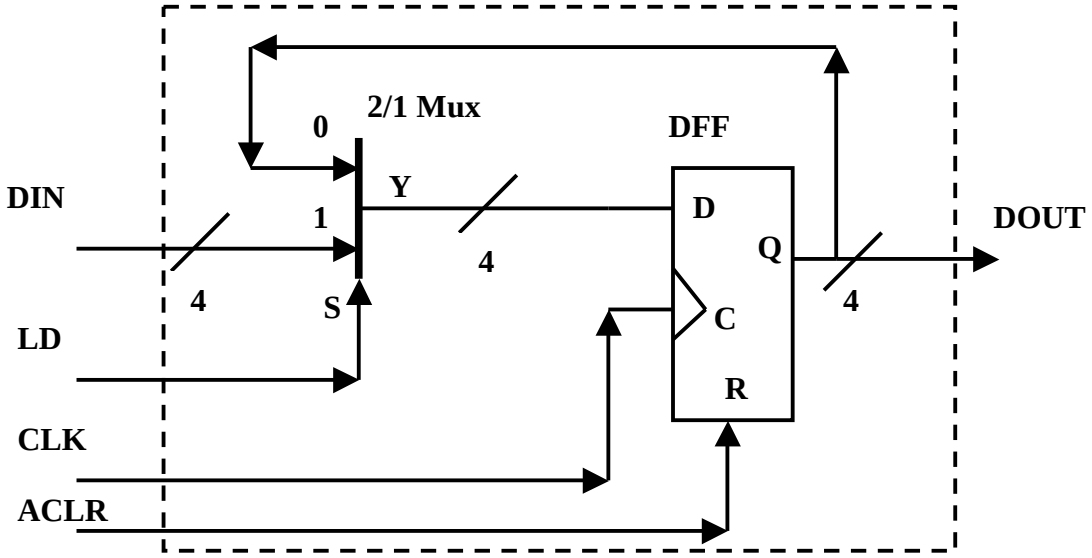
Or in VHDL: Y <= B when (S = '0') else A;

The pinout of the 2/1 4-bit Mux is:



II. 4-Bit Register

Use the devices listed above to implement the 4-bit register shown below.



The details of the schematic are for you to determine!!!. You may use all or some of the integrated circuits listed in Section I.

A. Connect the DIN 4-bit bus to data switches and verify that register can be loaded, and can be asynchronously cleared.

B. Modify the circuit by taking DOUT[0]' (use the Q'output on one of your 74LS74s) and connect this to DIN[0]. This will cause the DOUT[0] value to flip each time the register is loaded. Set LD = 1, and apply a 1 MHz clock to the Clock input. Use the oscilloscope and measure the delay from the rising Clock edge on your least significant DFF to a stable value at the D-input of the least significant DFF. Measure this value for both rising and falling waveforms at the D-input. Compare this value against a computed delay value based upon your schematic and datasheet delay values. This measurement can also be accomplished using the oscilloscope in single capture mode. First, calibrate Channel 1 by connecting CH1 to the 1 Mhz clock and using the AUTOSET button. Then, connect CH1 to the single PULSE switch on the test box (and also connect the clock input of your circuit to this switch). Use the scope TRIGGER menu, and set the trigger mode to SINGLE, RISING EDGE. Use CH2 to monitor the D-input of the LSB DFF. Press the PULSE button once, and the scope should trigger on the rising edge of the pulse, with CH1 capturing the pulse, and CH2 capturing the D-input waveform.

C. The delay measured in Part B (from the rising clk edge to a stable value at the D-input of the least Significant DFF) is actually the SUM of two delays: 1) the delay

through the DFF and 2)the delay through the 2/1 Mux. Use the oscilloscope to measure the delay through the DFF (from the rising clock edge to the Q output). Use the oscilloscope to measure the delay through the 2/1 mux (LSB DIN value to LSB DOUT value). Compare the sum of these two delays to the total delay measured in Part B.

III. Report

A. Give a complete schematic of your design.
B. Show your analysis of the computed delay asked for in II.B. Show all delay values along the path from Clock input of the LSB DFF to the D-input of the DFF.
C. Compare the sum of the two delays measured in Part IIC to the single delay measured in PartIIB.
D. Add the worst case setup time for the D-input of the 74LS74 to the delay measured in B, and take the inverse of this delay to find a clock frequency (in MHz). This is the fastest clock frequency that this circuit could be reliably clocked.

PRE LAB DATA SHEET TA CHECKOFF _____

1. The ZIP archive for this lab has a schematic called "p1.gdf" that implements a 4-bit register. A simulation of this circuit is in the waveform file called "p1.scf". Examine the waveform file and answer the following questions:

    a. From the waveform file, what is the delay through the 2/1 mux? _____ns.
    On a printout of this waveform, mark where you calculate or measure this delay. Use the 'Zoom' feature of the waveform editor to zoom in on portions of the waveform in order to get accurate delays.

    b. From the waveform file, what is the delay through the DFF (rising clock edge to output). _____ ns.
    On a printout of this waveform, mark where you calculate or measure this delay.

    c. On the waveform file, the LD line is asserted at 740 ns yet the output of the register does not change. Why is this???? Explain in detail.

    d. On the waveform file, what is the delay from the assertion of the asynchronous clear line to the output going to '0'? _____ ns
    Mark on your waveform where you calculate this value.

    e. These delays will NOT match the datasheet delays for the PLD and your 7474 because the programmable hardware assumed by Altera does not have the same timing characteristics as your PLD, 7474 device.

    Locate data sheets for your PLD and 7474 device and record the following delays:

    PLD (Tpd) _____ ns

    7474 T Clk to Q _____ ns

    7474 T setup _____ ns

    Calculate Maximum clock frequency as (1/ (Tpd + Tclk2Q + Tsu)
    _____ Mhz (give answer in Mhz)

2. Draw a detailed schematic for your 4-bit register using the devices given.

LAB DATA SHEET

A. Working 4-bit register (both synchronous load and asychronous clear demonstrated)

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B. 1. Measured Clk to Rising D delay value for II.B _____ (in ns)

2. Measured Clk to Falling D delay value for II.B _____ (in ns)

3. Max Clock Frequency (1 / ((Max of B1,B2) +Tsu)) _____(in Mhz)

C. Sketch of waveforms in II.B showing measurement points

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D. 1. Measured Clk to Rising Q delay value for II.C _____ (in ns)

2. Measured 2/1 Mux delay (Rising) for II.C _____ (in ns)

3. Sum of 1 + 2 (compare this to B1 above) _____ (in ns)

4. Measured Clk to Falling Q delay value for II.C _____ (in ns)

5. Measured 2/1 Mux delay (Falling) for II.C _____ (in ns)

6. Sum of 4 + 5 (compare this to B2 above) _____ (in ns)

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