

# Introducing the Silicore VMEbus to PCI Bridge SoC

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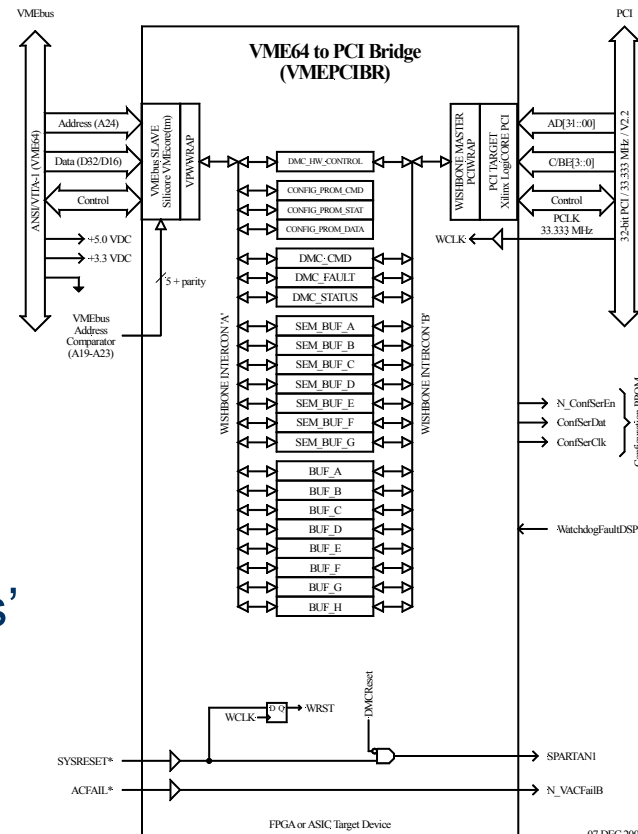
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# The Silicore VMEbus to PCI Bridge SoC

- It's a VMEbus to PCI Bridge System-on-Chip.
- It's a complete core system that's initially targeted to the Xilinx Spartan 2 FPGA, but can be easily moved to other FPGA and ASIC devices.
- It's available as free software under the LGPL public license. Available at: [www.silicore.net/VMEcore.htm](http://www.silicore.net/VMEcore.htm)

# Bridge Architecture

- VMEbus side:
  - Silicore VMEcore™
  - A24:D32:D16 slave
  - ANSI/VITA 1-1994
- PCI side
  - D32 target
  - 33 Mhz Xilinx LogiCore™
- Internal
  - 16-slot shared 'backplanes'
  - Dual WISHBONE SoC



## Based on Silicore's VMEcore™

- VMEcore™ was first introduced at the VSO conference in Vancouver, B.C. in July 1999 (3 ½ years ago).
- It provides a bridge between VMEbus and an internal bus called WISHBONE.
- WISHBONE is loosely based on VMEbus technology and marketplace.

# Low cost solution

- Most of the new VMEbus interface solutions cost \$200 - \$350 ea (100's).
- Features like 2eSST are great, but are overkill for many applications.
- The VMEbus to PCI bridge system is \$17 ea (100's) on Xilinx Spartan 2 FPGA's.

# The open source strategy

- The bridge SoC is provided as open source software a-la GNU/Linux. There is no charge to use, modify or share the code.
- Parts of the design were created or improved on several projects, over several years.
- Silicore adopted the open source (Red Hat) business model for semiconductor IP.

# Open source business model

- Traditional software (like Windows) is sold as a *product*. There, the fundamental ‘bargain’ is to trade a binary license for cash.
- Open source software (like Linux) is sold as a *service*. There, the fundamental ‘bargain’ is to trade a source code license for access to any enhanced derivative code.

# WISHBONE

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- The bridge uses dual WISHBONE internal buses.
- WISHBONE is the only open source System-on-Chip with readily available cores.
- WISHBONE is quite portable on FPGAs, and can be used on ASIC too.

# Advantages of portability

- Solves some very nasty parts obsolescence problems.
- Easily moved to devices with different physical characteristics (e.g. packages, voltages or temperature).
- Rock bottom prices when purchased under reverse auction bargaining processes.

# The WISHBONE technology

- It's a chip-level microcomputer bus that's loosely based on VMEbus (features, spec, etc.).
- It's a *soft system* that's usually described with hardware description languages such as VHDL or Verilog.
- WISHBONE has already spawned two software marketplaces: open source and conventional.

# The WISHBONE marketplace

- WISHBONE was adopted in 2001 by the on-line group at [www.opencores.org](http://www.opencores.org). They create semiconductor IP using open source software techniques (e.g. GNU/Linux).
- We're starting to see a commercial marketplace emerge too. Examples: various core vendors and Altium's Nexar tools.

# OpenCores.org

- Jan 2001: OpenCores adopts WISHBONE
- Apr 2003: The first publicly disclosed SoC based on WISHBONE is released (VOXI/Sweden).
- All of this infrastructure was built in just 27 months...with volunteer labor.
- The process improved WISHBONE, too.

# Long term strategy

- One long term strategy is to create VMEbus interface solutions based on the Apache Software Foundation model ([www.apache.org](http://www.apache.org)).
- The bridge core can be used as seed code.
- Silicore and Critia Computer (Ken Boyette) are forming the OpenVME Project for this purpose.

# The OpenVME Project

- Three linked objectives:
  - Modular synthesize core development
  - Unified software source code development
  - Test and development platform
- Now soliciting help from companies, groups and individuals for this purpose. If interested contact Wade Peterson or Ken Boyette.