Department of Electrical and Computer Engineering
COEN 6501 Dec. 8, 2011
Answer all Questions. All Questions carry equal marks
Exam Duration 3 hour
No books or papers are allowed. Lecturer: Asim J. Al-Khalili

Question 1

2 a. List programming techniques used in FPGAs and describe briefly two of these techniques.
b. Design a full adder and implement it:
2 b.1. Using 2:1 MUXs only. All inputs should be of non-inverting type.
3 b.2 Using 4 input MUXs only.
3 b.3 Using look up tables.

Question 2

Using Booth algorithm, design a circuit to implement the following function:

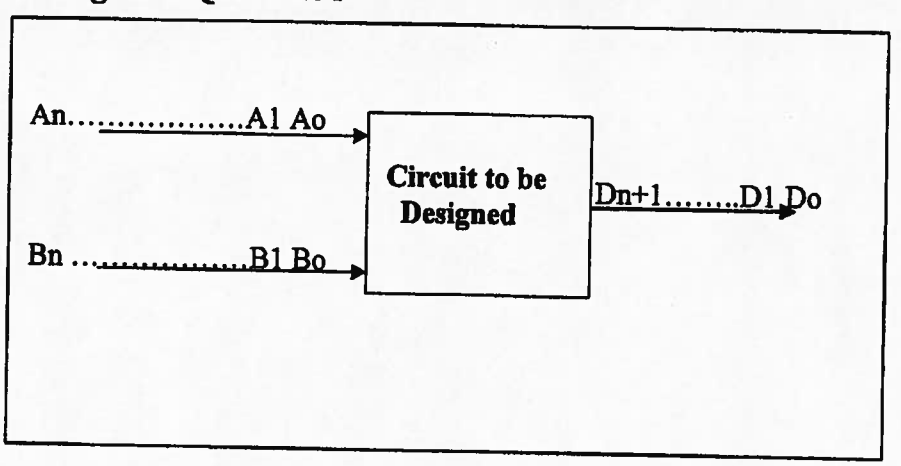
$F=N^2-3$ $N=-5$

Evaluate your design in terms of speed and area

Question 3

Two unsigned binary numbers are arriving on lines A and B. It is required to subtract the numbers (A-B) and produce the difference at output line D. Design the **sequential circuit *starting with a state diagram***

Fig. 1 of Question 3



Question 4

a. Identify and list all possible paths of the circuit.
b. Determine the maximum speed of operation at typical conditions for the circuit shown in Fig. 2 below. Timing parameters for all components are listed in Table 1. Assume skew is zero
c. The circuit is implemented on a die which is packaged in a ceramic DIP with a thermal resistance of 30°C/W. Calculate the drop in maximum speed of operation if the die dissipates a power of 2Watts at an ambient temperature of 40°C. Assume Θ=35 C/W and M=1.5. Assume a voltage variation of ±10%

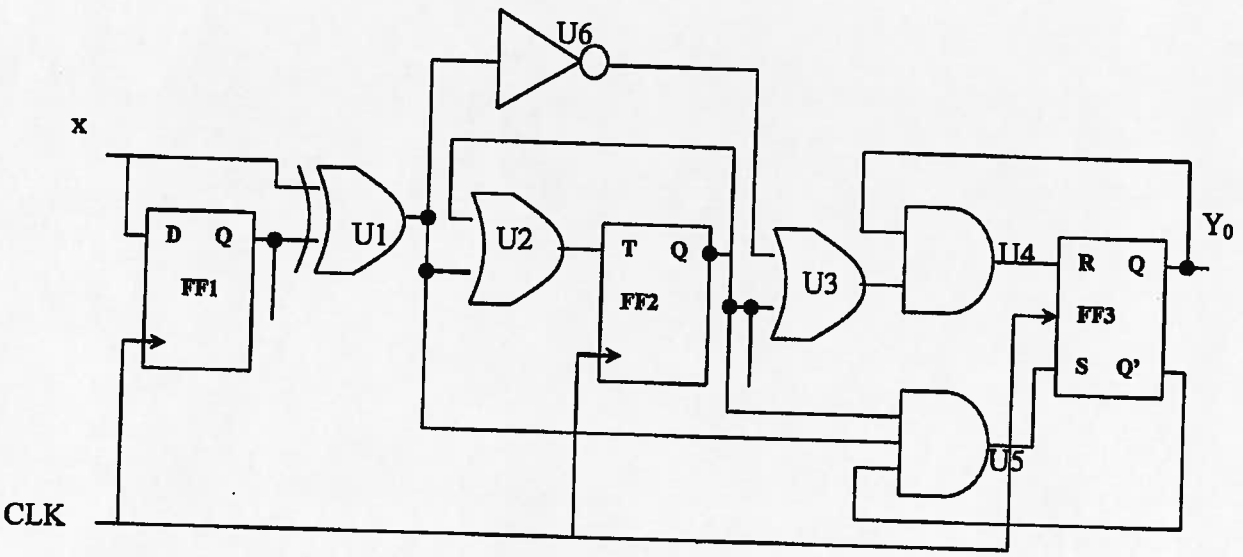


Figure 2

Component	Tp (ns)	Input Loading (UL)	K2 ns/fo	K1 ns/UL
Inverter	0.15	1	0.1	0.15
AND/XOR/OR	0.25	2	0.15	0.05
AND (3 input)	0.5	1.5	0.2	0.1
Flip Flops, (CK to Q) Tsu=1 ns, t_h = 0.5ns	1.5	2	0.25	0.2

$Td = \left((Tp + K1\sum Ni + K2\,ML) * K'\right)$, $K' = K_T * K_V * K$ $KT = \left(\frac{T2}{T1}\right)1.5$,

$T_J = T_{amb} + \Phi J_a * P_d$, $K_V = \frac{1}{1 + 0.01 * fv}$

Question 5

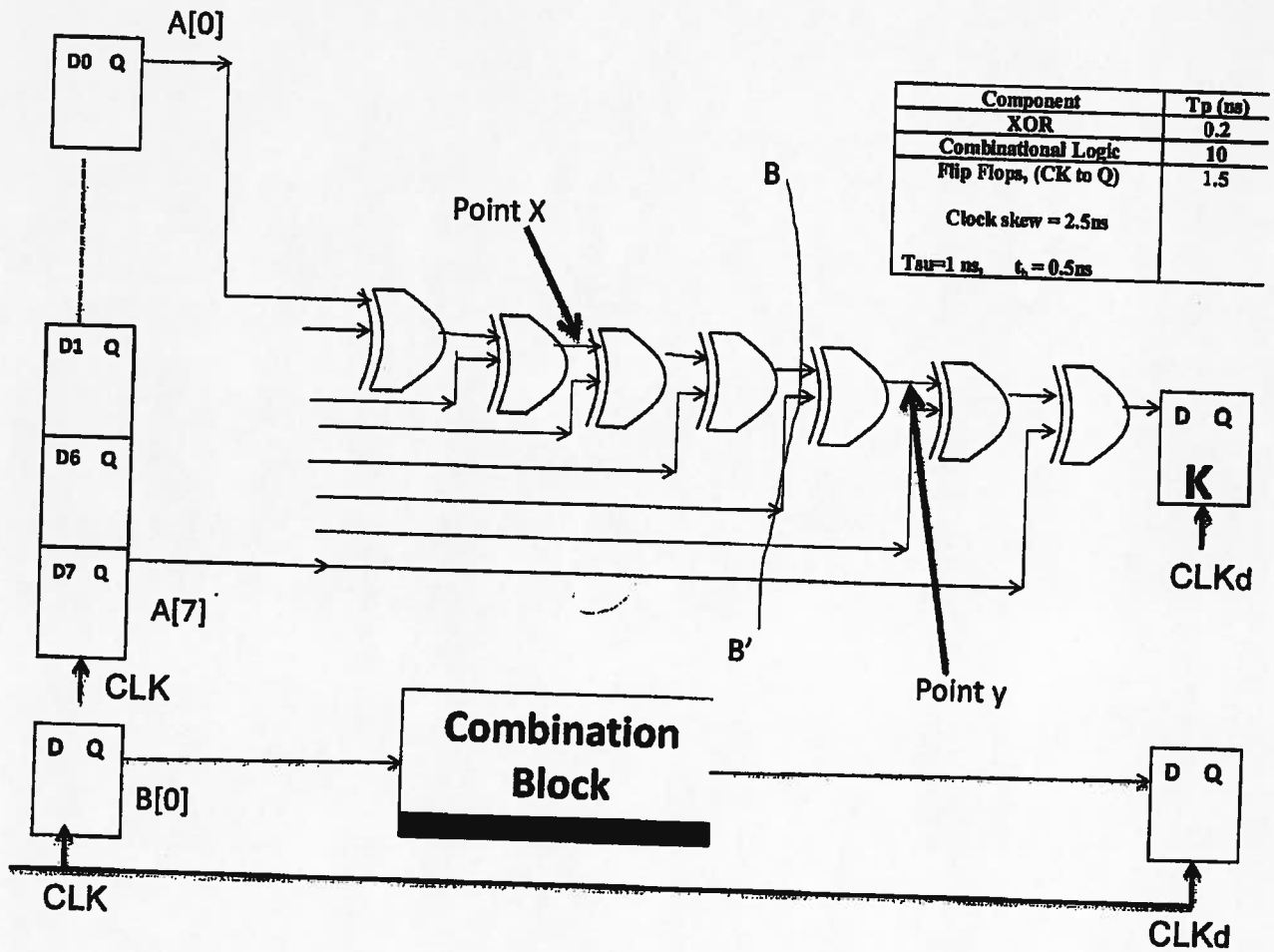
A registered parity checker is shown in Fig. below. The timing parameters for all components are listed in Table below.

a. Determine the maximum frequency of operation

b. Determine the minimum slack time for the hold time for F/F K.

c. All inputs Do to D7 and D arrive at the input of the FFs at time "-∞". First clock edge arrives at time "0". Determine "Required time" and "Arrival time" at points X and Y.

d. Determine the maximum frequency of operation if a pipeline is inserted at B-B', assuming zero clock skew.

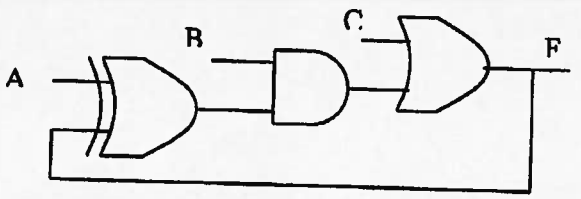


Component	Tp (ns)
XOR	0.2
Combinational Logic	10
Flip Flops, (CK to Q)	1.5
Clock skew = 2.5ns	
Tsu=1 ns, t_h = 0.5ns	

Question 6

For the circuit shown below,

a) Write a structural VHDL code for the entity .



b) For the VHDL code below draw the circuit, identifying all ports and signals clearly.
Can you deduce the circuit operation?
What libraries we would need to include for the code to operate correctly?

```
entity circuit is
 port(a: in BIT_VECTOR (7 downto 0)
       out1: out BIT ) ;
      end circuit;
  architecture structural of circuit is
    signal sig1: BIT_VECTOR (1 to 6);
      begin
          for i in 0  to 6 generate
 if i=0 generate --
              sig1 <= a(i) xor a(i+1);
          end generate;  -- i=0 case
if ( i >=1 and i <= 5) generate
sig1(i+1) <= sig1(i) xor a(i+1);
end generate;  -- 1< i <5 case
if i=6 generate
out1 <= sig1(i) xor a (i+1);
end generate;  -- i=6 case
end generate;
 end structural;
```

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a) EEPROM, EPROM, SRAM, PLA, PAL, PLDs are some programming techniques in FPGAs.

One such technique is the EEPROM technique. In this technique the program will saved on a non-volatile memory so that there is no to replace the PROM, rather re-program the PROM electronically on the board directly.

One other is SRAM technique. SRAMs are volatile memory, however they are fast and easily re-programmable, however they are expensive. Advantage immediate on board programming disadvantages are the fact that they are volatile, so, when power is turned off they loose their value.

b) A full adder design

a	b	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \bar{a}\bar{b}c_{in} + \bar{a}b\bar{c}_{in} + a\bar{b}\bar{c}_{in} + abc_{in}$

$C_{out} = \bar{a}bc_{in} + a\bar{b}c_{in} + ab$

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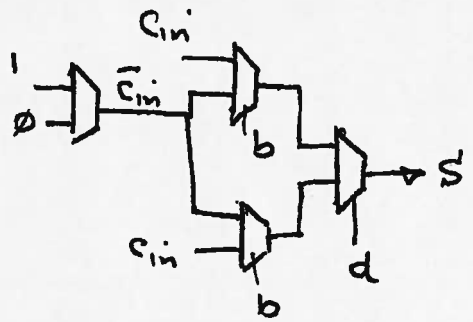
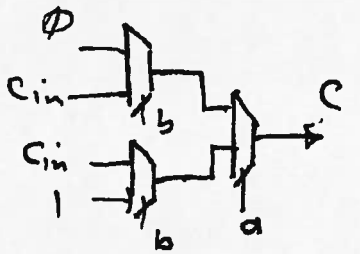
b1)

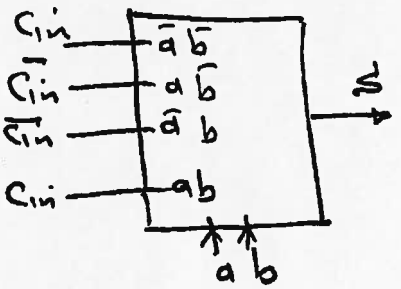


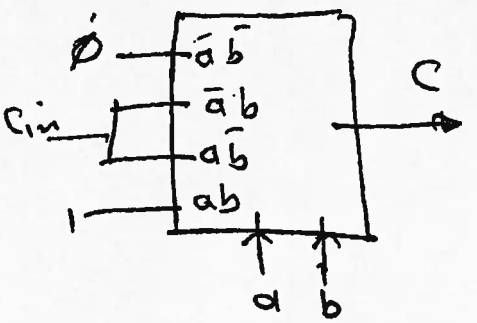
$$S = \bar{a}(\bar{b}c_{in} + b\bar{c}_{in}) + a(\bar{b}\bar{c}_{in} + bc_{in})$$



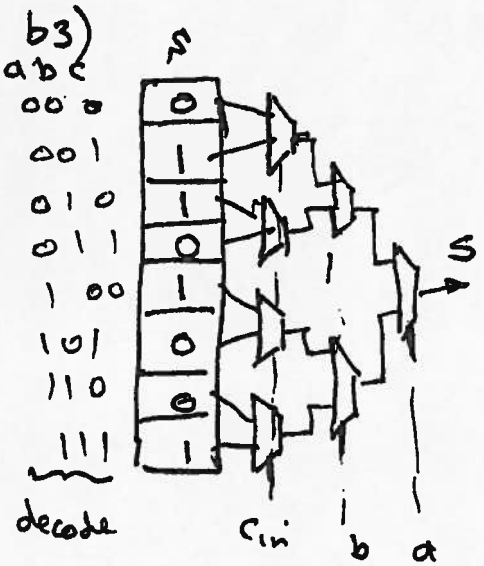
$$C = \bar{a}(bc_{in} + 0) + a(\bar{b}c_{in} + b)$$

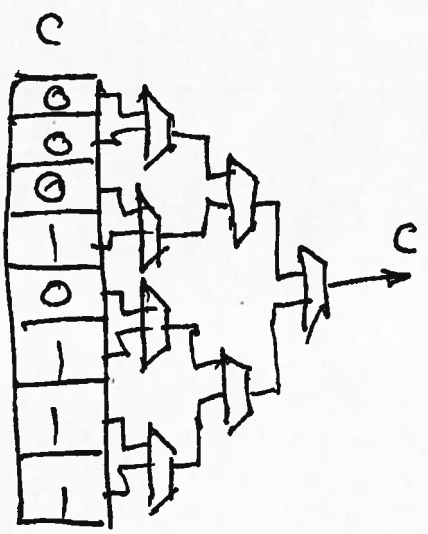
b2





b3)





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$N = n_3\ n_2\ n_1\ n_0$

$-3 = 1101$ 2's Complement form

$(-5)^2 = (5)^2$ Always +ve no need for Conversion

$$\begin{array}{r} 0101 \\ 0\ 1\ 0\ 1\ 0 \\ \hline 0\ 0\ 0\ 1\ 0\ 1 \\ 0\ 1\ 0\ 1\ 0\ 0 \\ \hline 0\ 1\ 1\ 0\ 0\ 1 \\ 1\ 1\ 1\ 1\ 0\ 1 \\ \hline 0\ 0\ 0\ 1\ 1\ 0 \end{array}$$

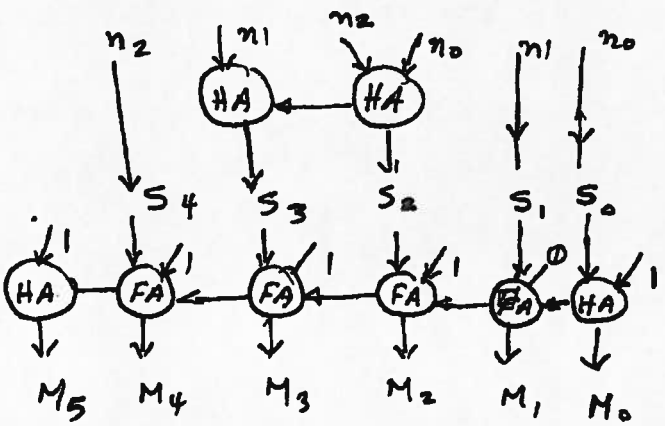
Encoding Booth

$n_3\ n_2\ n_1\ n_0$
$n_3\ n_0\ n_1\ n_0$
$n_2 \cdot n_1\ n_2 \oplus n_3\ n_0$
Carry n_0

$S_5 S_4 S_3 S_2 S_1 S_0 = 5*5 = 25$

$+ (-3)$

$\cdots - 22$



5 * 5

+ (-3)

Speed $2\tau_{HA} + 4\tau_{FA}$

Area $4A_{FA} + 4A_{HA}$

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a) Paths

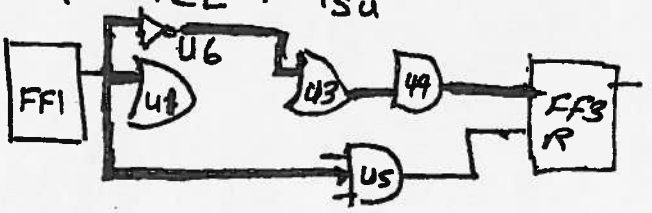
1. FF1 → U1 → U2 → FF2
2. FF1 → U1 → U5 → FF3
3. FF1 → U1 → U6 → U3 → U4 → FF3
4. FF2 → U2 → FF2
5. FF2 → U3 → U4 → FF3
6. FF2 → U5 → FF3
7. FF3 → U4 → FF3
8. FF3 → U5 → FF3
9. ~~FF3 → U4 → FF3~~

It seems path 2 has the largest delay and is the critical path

" 3 " also " " . . . . . .

Calculations for both, show that they are equal

$T = T_{CQ} + T_{CL} + T_{su}$



$$T = \overbrace{1.5 + 0.2(2) + 0.25}^{FF} + \overbrace{0.25 + 0.05(1+2+1.5) + 0.15\times 3}^{U1} + \overbrace{0.15 + 0.15(2) + 0.1}^{U6} + \overbrace{0.25 + 0.05(2) + 0.15}^{U3} + \overbrace{0.15 + 0.15\times 2 + 0.15}^{U4} + T_{setup}$$

$$= 5.625 \text{ ns}$$

$$\text{frequency} = \frac{1}{T} = 177 \text{ MHz}$$

Now Temp. Effects

$$\frac{T_J - T_A}{\theta_{JA}} = 2 \qquad T_J = 2 * 30 + T_A = 100^{\circ}C$$

$$K_T = \left(\frac{T_J + 273}{T_A + 273}\right)^{-1.5} = \left(\frac{100+273}{40+273}\right)^{-1.5} = 1.3$$

$$K_V = \frac{1}{1+0.1} = \frac{1}{0.9} = 1.43 = 1.11$$

$$K = K_T * K_V = 1.3 * 1.11 = 1.43$$

$$\text{frequency} = \frac{177}{1.43} = 124 \text{ MHz}.$$

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a) $T = t_{cQ} + t_{C} + t_{su} - t_{cs}$

$T = 1.5 + 10 + 1 - 2.5 = 10\,ns$

$\text{frequency} = \frac{1}{10} = 100\ MHz$

Since the combinational logic delay $10\,ns > 7 * 0.2$ then this is the critical path

b) To calculate the hold time slack we calculate the shortest path

Shortest path $D_7 \rightarrow 7\,XOR_S \rightarrow D_K$

$T' = 1.5 + 0.2 * 7 = 2.9\,ns$

$T_{hold\ slack} = T' - 0.5 - 2.5 = 2.9 - 3.0 = -0.1\,ns$

c)

	Arrival Time t_{cQ} + n * XOR delay	Required Time $T + t_{cs} - t_{su} - n * XOR\ delay$
X	$1.5 + 0.2 \times 2 = 1.9\,ns$	$10 + 2.5 - 1 - 5 * 0.2 = 10.5\,ns$
Y	$1.5 + 0.2 \times 5 = 2.5\,ns$	$10 + 2.5 - 1 - 2 * 0.2 = 11.1\,ns$

d) The insertion of the pipeline has no effect because it is in short path while $10\,ns >> 1.4\,ns$, but removal of the clock skew has an effect which will reduce the clock frequency

$T = 1.5 + 10 + 1 - t_{cs}^{0} = 12.5$

$f_{max} = 80\ MHz$

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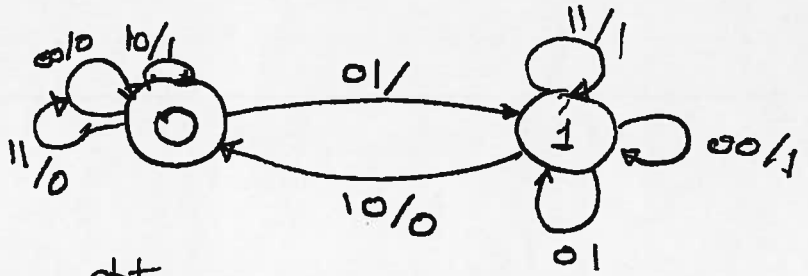
Two states Borrow & No Borrow, with {two inputs A, B & {2 outputs D, Bo



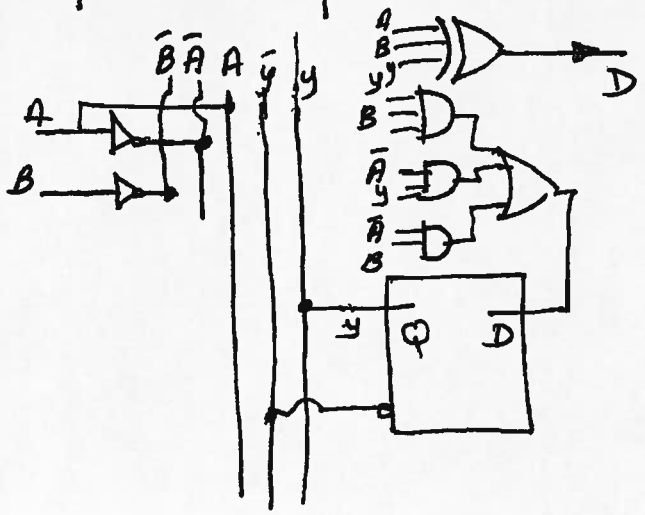
No Borrow = "0" state with Borrow = "1" state

Present State

y	y+ 00	01	11	10	D 00	01	11	10
0	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0

$y^+ = D_{inputs} = yB + y\bar{A} + \bar{A}B$

$D_{diffc} = y \oplus A \oplus B$



Q6) Dec 2011 COEN 6501

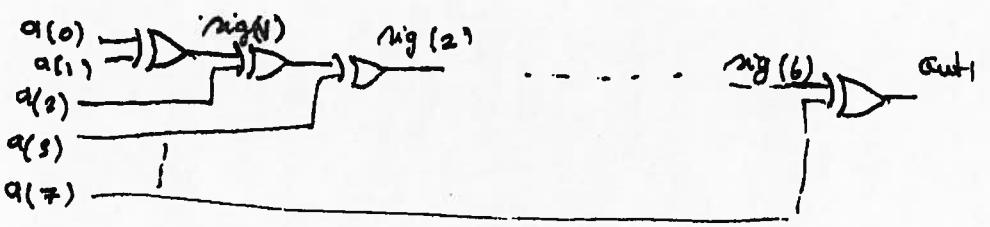
a)

```
entity exam is                          -- or std_logic
Port (A, B, C : in BIT; F : out Bit)
end exam;

Architecture Question of exam is
    component and2 port (a, b : in Bit; c : out Bit); end component;
    component or2  port (a, b : in Bit; c : out Bit); end component;
    component xor2 port (a, b : in Bit; c : out Bit); end component;
    signal temp1, temp2 : Bit;
begin
    A1 : and2 portmap (a, b, temp1);
    A2 : or2  portmap (c, temp2, F);
    A3 : xor2 portmap (A, F, temp1);
end Question;
```

b) Code correction: These are underlined below:

```
Port (a : in Bit_vector (7 downto 0);
sig1 (1) <= a(i) xOR a(i+1)
```



The library code is

```
library STD;
use STD.all
```

The circuit is even parity checker