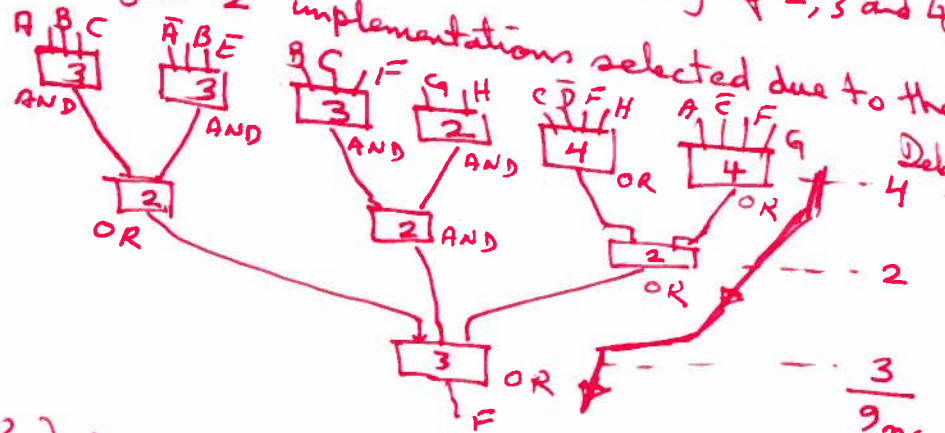
Q 1 COEN 6501 Dec 9, 2013

a) FPGAs have several advantages some are:

a) Ease of prototyping
b) Fast Prototyping
c) Low cost of prototyping
d) Re-programmability
e) Availability of variety of FPGAs with embedded units
f) Availability and friendlyness of tools
h) Fast testing of the circuit.

b) $F(A,B,C,D,E,F,G,H) = ABC + \bar{A}BE + BCFGH + CD'FH + A\bar{C}FG$

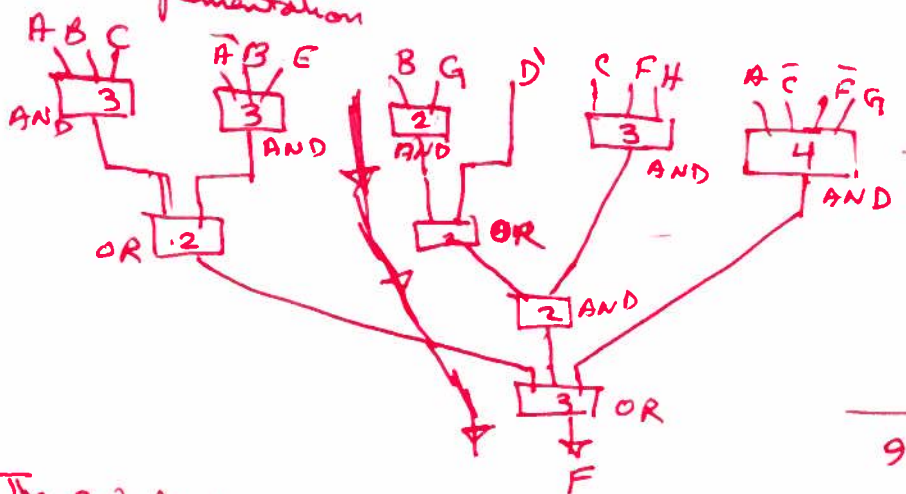
F can be implemented with a variety of 2, 3 and 4 variable LUT. In here we give 2 implementations selected due to their lowest delay



Delay
4
2
3
9 ns

Area
4 * 3 LUT
4 * 2 LUT
2 * 4 LUT
124 mm²

2nd Implementation



Delay
2
2
2
3
9 ns

Area
4 X 3 LUT
4 * 2 LUT
1 * 4 LUT
98 m²

The 2nd Implementation has the same delay, but a better Area.

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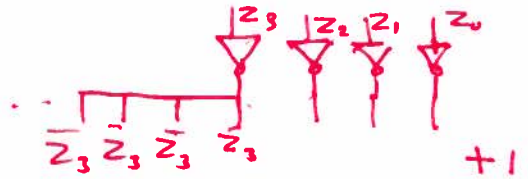
Q_2

$X.Y - Z = (X.Y) + (-Z)$

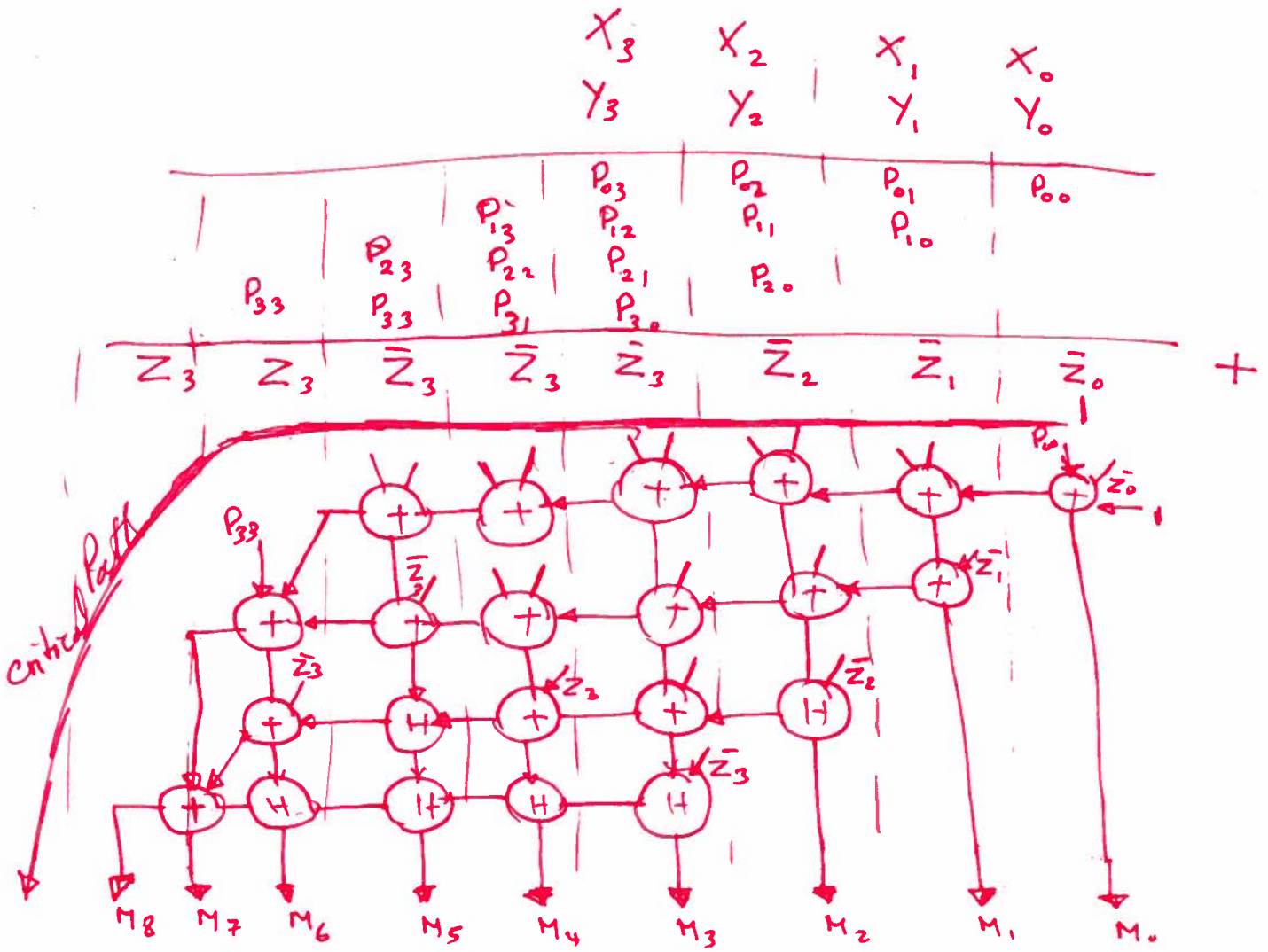
$Z = Z_3\ Z_2\ Z_1\ Z_0$

$-Z = \{\bar{Z}_3\ \bar{Z}_2\ \bar{Z}_1\ \bar{Z}_0$

extension $\cdots \bar{Z}_3 \bar{Z}_3 \bar{Z}_3$ $\}$ 1 +



Z is inverted and '1' is added to get its -ve value and NOT XORed since we want is -ve.



Critical Path = $8\tau_f$ + 7AND

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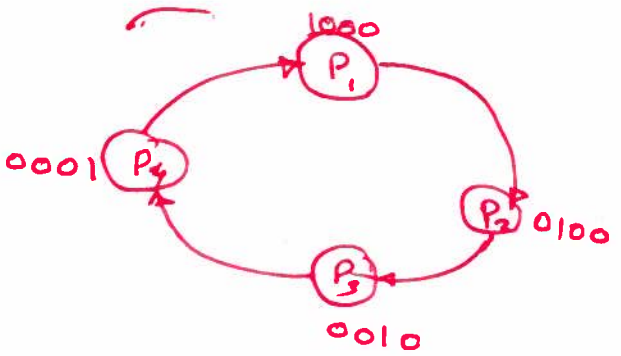
Q3



Present state $y_3 y_2 y_1 y_0$	Next state $y_3^+ y_2^+ y_1^+ y_0^+$	
P_1 1000	0001	P_1^+
P_2 0100	1000	P_2^+
P_3 0010	0100	P_3^+
P_4 0001	0010	P_4^+

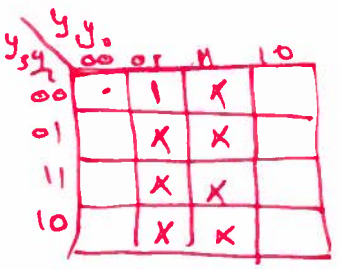
i.e from the Table above

$P_2^+ = P_3$ $\quad y_3^+ = y_0$

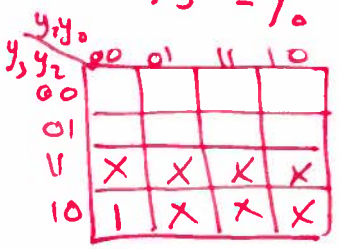
$P_3^+ = P_4$ $\quad y_2^+ = y_3$

$P_4^+ = P_1$ $\quad y_1^+ = y_2$

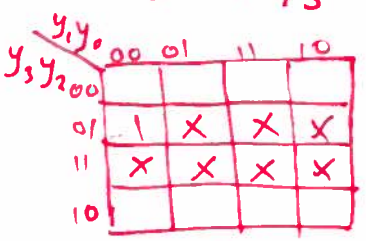
$P_1^+ = P_2$ $\quad y_0^+ = y_1$



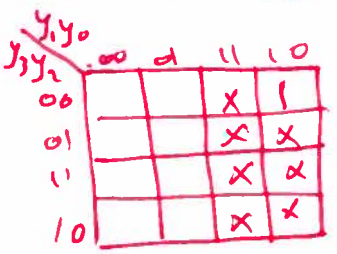
$Y_3^+ = Y_0$



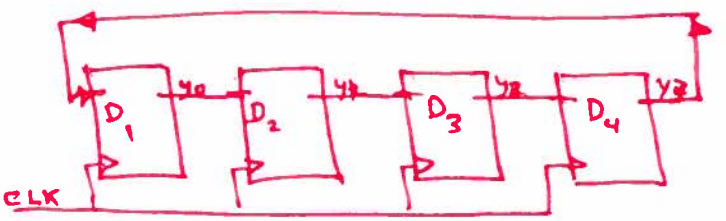
$Y_2^+ = Y_3$



$Y_1^+ = Y_2$



$Y_0^+ = Y_1$



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a) There are 6 paths

Path 1 : U1 - U2 - U4 - U6

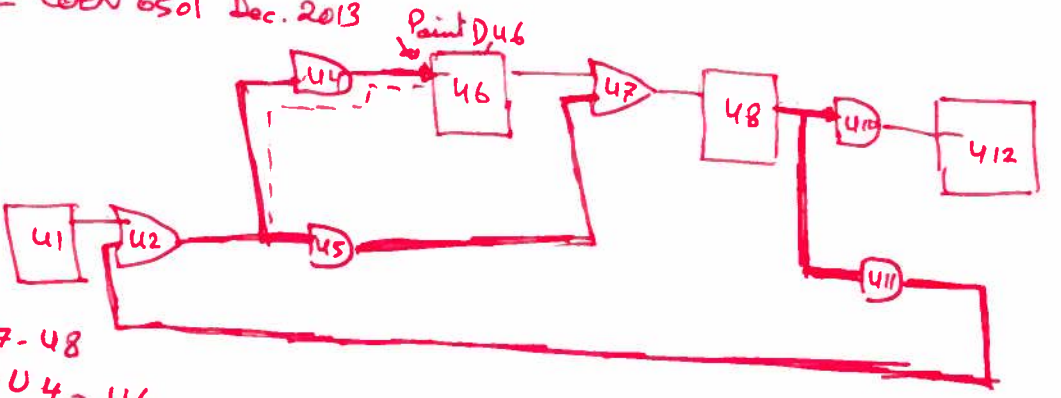
Path 2 : U6 - U7 - U8

Path 3 : U8 - U10 - U12

Path 4 : U1 - U2 - U5 - U7 - U8

Path 5 : U8 - U11 - U2 - U4 - U6

Path 6 : U8 - U11 - U2 - U5 - U7 - U8 ← By inspection and calculation Critical Path



$C_{L6} = \underbrace{0.2\,(1.5+1.5)}_{U8} + \underbrace{2 + 0.25*1.5}_{U11} + \underbrace{2.5 + 0.25*(1.5+1.5)}_{U2} + \underbrace{2.0 + 0.25*1.5}_{U5} + \underbrace{2.5 + 0.25*1}_{U7} = 11.35\,ns$

$T_{max} = \gamma_{int\,ff} + C_L + t_{set\text{-}up} = 3 + 11.35 + 1.5 = 15.85\,ns$ so $f_{max} = \frac{1}{T} = \frac{1}{15.85\,ns} = 63.1\,MHz$

b) Path delay @ point D, U6 which is Path 5

$0.2*(1.5+1.5) + 2 + 0.25*1.5 + 2.5 + 0.25(1.5+1.5) + 2*0.25*1 = 8.47\,ns$

$T_{set\,up\,slack} = (T_{max} - T_{su}) - T' = 15.85 - 1.5 - 11.47 = 0.875\,ns$

T_{hold} @ point D U6 is $= \gamma_{int\,ff} + 8.47\,ns = 11.47 = T'$

$t_{h\,max} < t_{cq\,min} + t_{CL\,min} - t_{cs\,max}$

$t_{CL\,min}$ is Path 1 delay, $t_{cq\,min} = 3$ $t_{cs\,max} = 0$ & $t_{Path\,1} = 8.65$

$\therefore t_h = 3 + 8.65 - 0 = 14.47$

t_h slack $= 14.67 - 0.5 = 13.97\,ns$

c) When clock skew is introduced between U1 & the rest we calculate the changes to the path. Path 4 is the longest path

$T_{path\,4} = \underbrace{(0.2)\,1.5}_{U8} + \underbrace{2 + 0.25\,(1.5+1.5)}_{U11} + \underbrace{2 + 0.25*1.5}_{U2} + \underbrace{2.5 + 0.25*1}_{U5} + \underbrace{\gamma_{int\,ff} + t_{su}}_{U7} = 13.175 + 3.5 = 16.67\,ns$

Noncritical path has been introduced $T_{path\,4} > T_{path\,6}$

This is the added delay at the input of U_2 ↑ delay

since CLK of other FFs is taken as a reference

New frequency $= \frac{1}{16.67} = 59.981\,MHz$

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Q5

b) Typical Delays

$t_{NAND} = 0.25 + 0.03 * 1.5 = 0.295$ ns
$t_{XNOR} = 0.4 + 0.05 * 2 = 0.5$ ns
$t_{MUX} = 0.3 + 0.1 \times 2 = 0.5$ ns
$t_{FF} = 0.5 + 0.07 * 1.5 = 0.605$ ns
} @ ambient temp of 27°C

Delay variations

$k_V = \frac{1}{1 + 0.01 f_s} = \frac{1}{1 \pm 0.01 \times 10} = 1.11, 0.909$ Voltage variation

$k_T = t_a + \theta_{Ja} * P_s$ -

$(T_2)_{min} = -55 + 30 * 3 = 35^\circ C + 273 = 308^\circ K$
$(T_1)_{max} = 125 + 30 * 3 = 215^\circ C + 273 = 488^\circ K$
} Junction Temp Variation

$k_{T min} = \left(\frac{308}{27+273}\right)^{1.5} = +1.05$

$k_{T max} = \left(\frac{488}{27+273}\right)^{1.5} = +2.09$
} De-rating, Temp Variation

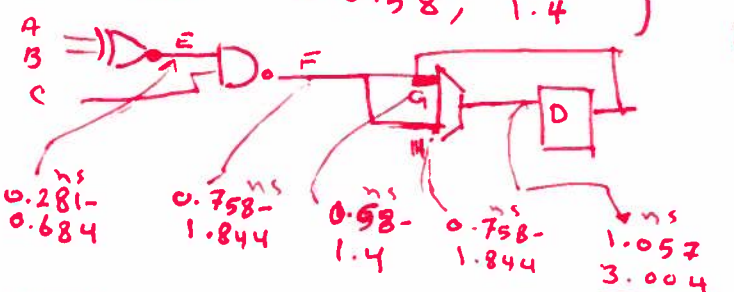
Composite De-rating factor $k' = k_V * k_T$

$k'_{min} = 0.909 * 1.05 = 0.954$
$k'_{max} = 1.11 * 2.09 = 2.09$

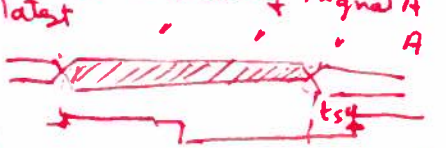
Min/Max Delay

	ns	ns
t_{NAND} =	0.281,	0.684
t_{XNOR} =	0.477,	1.16
t_{MUX} =	0.477,	1.16
t_{FF} =	0.58,	1.4

} Min, Max Delay of the Gates used in Fig Q



← earliest arrival of signal A
← latest



b) Total Period $T = \tau_{CQ_{max}} + \tau_{CL_{max}} + T_{SU_{max}} - t_{CS_{min}}$

$T_{max} = 1.4 + 3.004 + 0.2 - 0 = 4.$ ... $f = \frac{1}{\quad}$

Q6

a) There is many ways of writing this piece code here is just a simple example:

```
library IEEE;
use ieee.std_logic_1164.all;
entity exam_Circuit is
Port ( A, B : in std_logic ; O1, O2 : out std_logic );
End exam_circuit

architecture structural of exam_circuit is
Component decoder 2 to 4
          Port ( a, b : std_logic ; d1, d2, d3, d4 : out std_logic);
end Component decoder 2 to 4;
Component AND_Gate
          Port ( in1, in2 : in std_logic; out1 : out std_logic);
end Component AND_Gate;
Component OR_Gate
          Port ( in1, in2 : in std_logic; out1 : out std_logic);
end Component OR_Gate;
Signal d1, d2, d3, d4 : std_logic ;
Begin
     dcoder1 : decoder 2 to 4 port map (A, B, d1, d2, d3, d4);
     AND1    : AND_Gate  Port map ( d1, d2, O1);
     OR1     : OR_Gate   Port map ( d3, d4, O2);
end structural
```

b)

```
L2   X,Y : in  std
L4   end Half_A_Com
L5   H_A_Behav
L7   -- signal
L8   Procom (X,Y)
L13  Problem of conversion X, Y
L17  end if
```