Configurable Logic Devices
A Market Overview and Introduction

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Introduction

Rapidly increasing mask costs and lengthening Application Specific IC (ASIC) design cycles necessitate new solutions to produce custom logic devices on time and on budget. As fewer companies can make a business case for cell-based ASIC designs, they revert to less-costly options or try to replace custom logic devices with off-the-shelf Application Specific Standard Products (ASSPs).

Field Programmable Gate Arrays (FPGAs) offer an alternative, but they come with significant drawbacks including limited performance and capacity, high unit costs and power consumption. This dilemma has caused a resurgence of gate-array style devices that are now being marketed as "Structured ASICs", in an attempt to address the shortcomings of standard cell ASICs.

The only way to deliver the required performance and meet market windows is to integrate ASIC and FPGA capabilities in the same device. Embedded FPGA will become a key enabling technology for future ASIC and System-on-Chip (SoC) designs, much like embedded memory and processors already are today.

Embedded FPGA technology enables the combination of the flexibility and time-to-market of FPGAs with the capacity and performance of an ASIC. The market for devices using this technology is forecast to skyrocket to over $650M in 2007 at a Compound Annual Growth Rate (CAGR) of 115% according to market research firm In-Stat/MDR.

The Alternatives & Tradeoffs

Traditional design approaches including ASICs and FPGAs and the recent introduction of Structured ASICs all address some of the needs, but have significant shortcomings in other areas:

- The ASIC Dilemma
  While ASICs provide a good price/performance trade-off once in production, the huge ASIC design, tool and mask costs are prohibitive for most companies who cannot afford to invest millions of dollars into EDA tools, training, and manufacturing. Rigid ASIC design flows, long manufacturing times and the hardwired implementation lack the flexibility needed to address fast moving or emerging market opportunities in a timely fashion. Also, many infrastructure applications mandate field upgradeability as a critical requirement.

The Alternatives & Tradeoffs (continued)

- Catch 22 for FPGAs
  FPGAs address the time-to market problem and lack of flexibility of ASICs and avoid the steep upfront investment in tools and non-recurring engineering (NRE) costs. But high FPGA unit costs prohibit their use in cost sensitive applications. High power consumption and low performance, combined with limited capacity are technical criteria that make the use of FPGAs in many applications impractical or economically unfeasible.

- Structured ASICs
  These devices look and work much like the well known gate arrays, using multiple metal layers for configuration, but do not offer a viable alternative. Structured Arrays utilize a gate array style design flow where the user has to submit the netlist or RTL to the ASIC vendor for timing closure and back end design, resulting in potentially lengthy timing closure cycles. Many of the proposed devices include hardwired functions such as embedded processors, which limit their applicability to specific vertical markets, and all fall short of providing FPGA-like flexibility.

Market Trends

Advanced 90 nm process technology will make things worse – or better, depending on the perspective. While mask charges will continue to increase and design and tooling costs spin out of control, every process node will make FPGA-based products more attractive. Silicon cost is no longer the main cost factor for the majority of products, as amortized NRE, packaging and test become the dominant cost drivers.

Looking back in history, disk storage used to limit the amount of data stored on a computer and mandated software efficiency. Then, the emergence of low-cost storage has enabled new approaches to programming, as software developers embraced modular object and library based development methodologies. While less efficient with respect to storage and CPU cycles, these methodologies have gained wide adoption and are the basis for continued innovation and rapid development today.

The equivalent trend is happening in chip design today, as larger designs are assembled from existing components, i.e. silicon intellectual property (IP) blocks. As the industry continues to drive silicon costs down and to increase the integration capabilities, the current focus on die area will give way to a focus on flexible implementations and short development cycles.

Once believed the panacea to lowering their component costs, most OEMs are now abandoning their internal Customer Owned Tooling (COT) flows and are reverting back to an ASIC style design flow, using outsourcing and traditional ASIC vendors and FPGAs wherever possible and economically feasible. Whenever designs require extreme performance, capacity or lowest power, standard cell ASICs will likely remain the technology of choice, as long as the volume and price points justify the business case and allow for the amortization of the large development expenses.

On the other end of the spectrum, FPGAs will continue to dominate prototyping and very low volume applications with some small devices creeping into higher production volumes.

Market Trends (continued)

For a growing number of designs however, neither of these options seems to work. Latest statistics show that about 50% of ASICs and virtually 100% of FPGA designs never exceed 100k lifetime units. The median design complexity currently is about 1.2M gates (800k logic and 400k memory).

Designs in this complexity range require the largest FPGAs, costing thousands of dollars. The result of these trends is a growing number of designs that cannot be addressed effectively with either ASIC or FPGA.

Figure 1. illustrates this market gap between FPGAs and standard cell ASICs in the volume range between 1,000 units to 100,000 units.

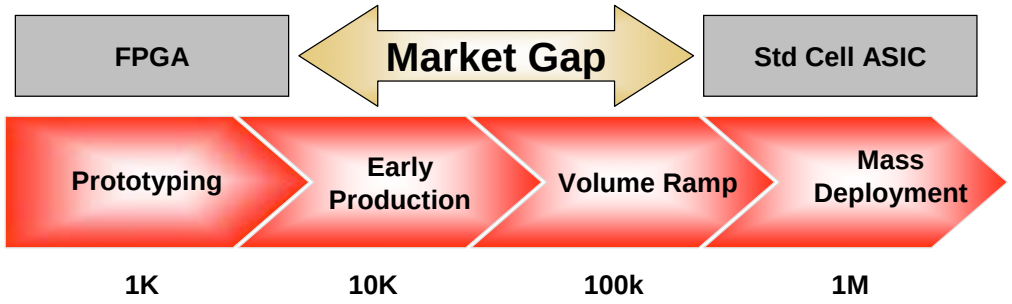

Figure 1. Market gap between FPGAs and ASICs

The Future is Hybrid

Today, the only way to achieve high integration efficiency and performance while providing flexibility on the system level is to combine discrete ASICs and FPGAs on a printed circuit board. However, this approach introduces a performance bottleneck between these devices,in addition to other issues such as high power consumption, large board space and high costs for the system implementation.

Embedded programmable logic technology enables the creation of flexible, yet cost-effective hybrid device platforms. The key challenge is to make this technology easy to deploy for the system designer. Integrating an FPGA block into a standard cell ASIC falls short of delivering on the promise of this technology as a major value proposition of FPGAs is lost with this approach, i.e. fast time to market.

Configurable Logic Devices

Configurable Logic Devices (CLDs) are a new class of digital semiconductor devices designed to eliminate the shortcomings of ASICs and FPGAs, providing designers with a new option to implement high-performance designs quickly and cost-effectively.

By using a combination of field-programmable and mask programmable logic, CLDs deliver superior performance and lower power and cost as compared to FPGAs. At the same time, they retain flexibility in the design where it matters.

Configurable Logic Devices (continued)

With a design cycle and an upfront investment comparable to an FPGA and the performance and capacity of an ASIC at a very attractive price point, CLDs are the device of choice for the future.

CLDs are ideally suited for a variety of applications including DSP and packet processing, and allow for fast time to volume at attractive price points. Design functions that are fixed or low-risk, such as data path functions are implemented in the efficient ASIC fabric, while high-risk blocks and functions that require field-upgradeability are placed into the on-chip FPGA fabric. This partitioning provides FPGA-like design cycles and flexibility, while achieving ASIC-like performance, power and cost.

Figure 2. shows a typical SoC block diagram that identifies the key areas requiring design flexibility to mitigate risk, enable fast derivatives, and provide protection against evolving standard and interoperability requirements.

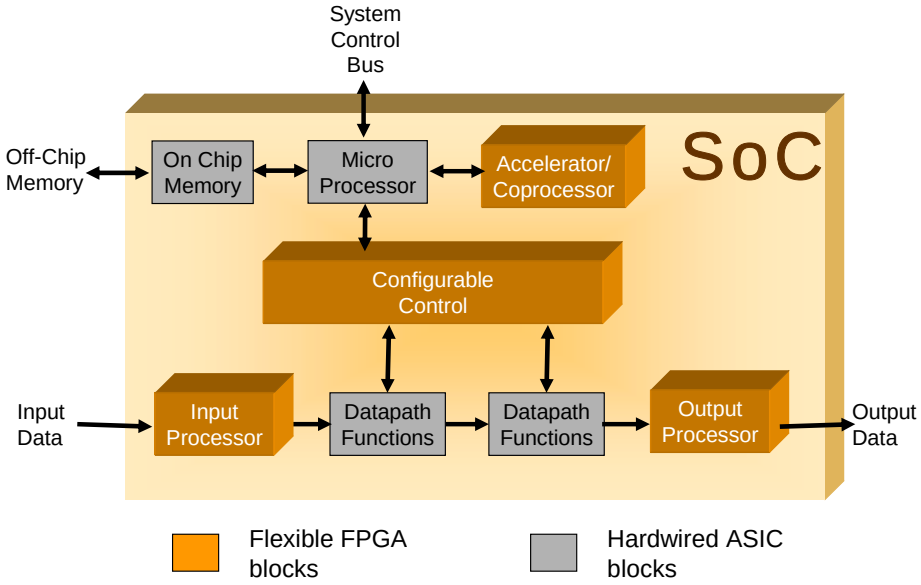

Figure 2. Partitioning between hardwired and flexible functions

In the past, designers were forced to partition their design into multiple devices to achieve the right trade-off between flexibility, performance, cost and power. This partitioning had to happen early in the design process to account for long ASIC design cycles. With this approach, the system partitioning was usually sub-optimal and could not be changed at a later time.

Configurable logic devices eliminate this issue and offer a new alternative for system designers to implement their designs and meet price/performance objectives, as markets continue to fragment and market windows shrink.

Gladiator™ CLD™ – The Solution

Gladiator CLD is a family of configurable logic devices combining the benefits of FPGAs and ASICs in a low-cost, yet versatile device. These benefits are achieved by using a combination of Leopard Logic's proprietary HyperBlox™ FP and MP fabrics, along with dedicated memories and Multiply-Accumulate (MAC) units. With a design cycle and an upfront investment comparable to an FPGA, Gladiator CLD delivers the performance and capacity of an ASIC at a very attractive price point. This results in the lowest Total Cost of Ownership (TCO) for products with unit volumes ranging from 1k to 100k units.

The performance and ease-of use of Gladiator CLD enables customers to instantly tap a vast array of existing IP components from prior designs or third parties. Leopard Logic is teaming up with leading IP providers to assure efficient access to best-in-class, silicon proven IP solutions for its target applications.

Conclusion

ASICs will not die anytime soon but customers and vendors will become even more selective as to where this technology makes sense. FPGAs on the other hand will keep their spot in prototyping and low-volume applications while vendors will continue to ride the process curve.

Figure 3. compares the different approaches with respect to cost and flexibility. Flexibility is measured as time to market (TTM) and turn-around time (TAT) required for incremental design changes.

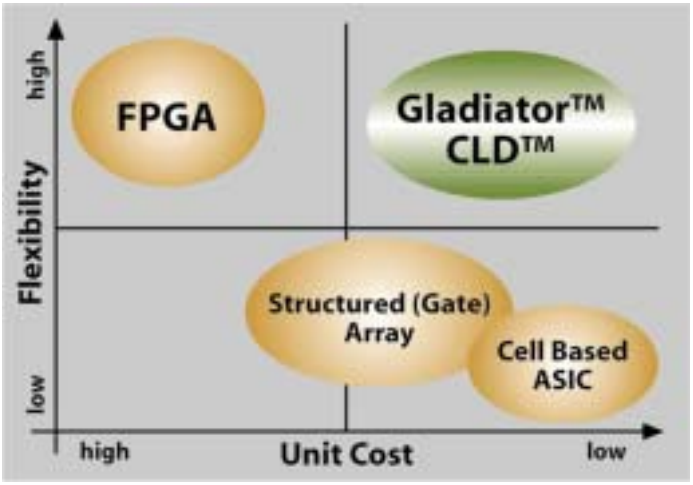

Figure 3. Flexibility/cost comparison

The key question is what happens to the growing number of designs that fall into the market gap. Structured ASICs may pick-up some of these designs as gate arrays did in the past, but the true gain will be realized by using configurable logic devices, which offer the most attractive trade-offs for many demanding applications.

Conclusion (continued)

Configurable Logic Devices allow users to tap into a wealth of existing IP blocks, proven methodologies and design tools. These devices allow instant design changes like FPGAs, while leveraging the more efficient ASIC logic for fixed blocks of a design. These characteristics make CLDs the ideal implementation platform for products that would otherwise fall into the market gap.

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