Get Ready
for the
Next Generation
Configurable
Logic Experience

Gladiator™

FPGA Flexibility
ASIC Efficiency

LEOPARD LOGIC, INC.

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Future Proof Your Design

System Design Requirements

Complex systems need a way to accommodate changes and update the system behavior during and even after manufacturing as the product matures. Today, the only way to achieve high integration efficiency and performance, while providing flexibility on the system level, is to combine Application Specific Integrated Circuit/Application Specific Standard Product (ASIC/ASSP) devices with standalone Field Programmable Gate Arrays (FPGAs) on a board.

This approach introduces a number of issues such as high power consumption and large board space, resulting in undesirably high costs for the system implementation.

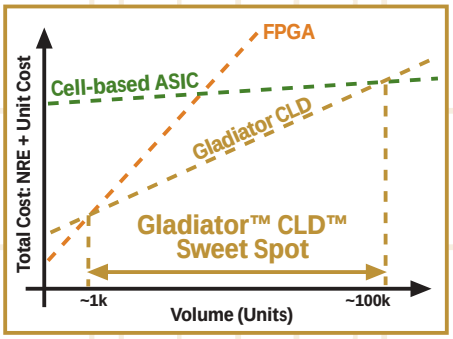
Leopard Logic is developing a new class of configurable logic device that addresses the critical integration issues currently faced by system designers, and that represents a significant advancement over legacy logic devices.

By combining ASIC and FPGA technologies in a single device and design environment, Leopard Logic's innovative solution allows instant design changes like FPGAs, while leveraging the more efficient ASIC logic for fixed blocks of a design. The design flow utilizes existing infrastructure and proven methodologies, while eliminating the need for lengthy back end processing and manufacturing as necessary for ASICs. As a result, system designers can create cost effective solutions that meet their performance, density and power objectives.

Today's Design Dilemma

Changing Standards and Interoperability Requirements

Technical standards such as communication protocols, data formats or bus interfaces are in a constant state of flux. Rapidly evolving specifications and changing market requirements cause invariable interoperability challenges. Designers have to address these changing requirements under stringent budget constraints, while having to meet ever shortening product development cycles.



"ASICs just don't work for many companies anymore because of escalating costs and extending development cycles. The FPGA market is profiting from this trend. Over the next several years, we see a fast growing market for hybrid devices that use a combination of hardwired logic and embedded FPGA fabrics."

Jerry Worchel,
Senior Analyst, In-Stat / MDR

Increasing Costs

Rapidly increasing mask costs and lengthening design cycles of ASICs necessitate new solutions to produce custom logic devices on-time and on-budget. This dilemma is driving the FPGA market today and has caused a resurgence of gate-array style devices that are now being marketed as "Structured ASICs".
As fewer companies can afford cell-based ASIC designs, they revert to less-costly options or try to replace custom logic devices with off-the-shelf ASSPs.

Elusive Time to Volume

Today's fast changing market place requires rapid product deployment in order to remain competitive. Latest statistics show that about 50% of ASICs never exceed 100k lifetime units and pinpoint the median design complexity at about 1.2M gates (800k logic and 400k memory).
Many ASICs take so long to build that the specifications are outdated by the time the devices are finally delivered, thus rendering them practically obsolete. On the other hand, while quick to market, FPGAs are not suitable for high-volume deployment.
The result is a growing number of system designers seeking viable alternatives to implement their logic designs.

"Moore's Law propels chip designs to higher levels of integration, and therefore complexity. 90 nanometer designs cost between $13 million to $30 million and take 18 to 24 months to complete. This lag time is not acceptable for most products in the new millennium. Markets fragment into finer and finer segments, while each ASIC, ASSP or System-on-Chip (SOC) gradually becomes more expensive and requires larger volumes to amortize the cost.

Charles Dilisio,
President, D-Side Advisors

With Gladiator™ CLD™

The Current Choices

ASICs: Prohibitive design, tool and mask costs – no flexibility

While ASICs provide a good price/performance trade-off once in production, the huge ASIC design, tool and mask costs are prohibitive for most companies who cannot afford to invest millions of dollars into EDA tools, training, and manufacturing. Rigid ASIC design flows, long manufacturing times and the hardwired implementation lack the flexibility needed to address fast moving or emerging market opportunities in a timely fashion.

FPGAs: High unit costs and power consumption – low efficiency

FPGAs address the time-to market problem and lack of flexibility of ASICs and avoid the steep upfront investment in tools and Non-Recurring Engineering (NRE) costs. But high FPGA unit costs prohibit their use in cost sensitive applications. High power consumption and low performance, combined with limited capacity are technical criteria that make the use of FPGAs in many applications impractical or economically unfeasible.

Structured (Gate) Arrays

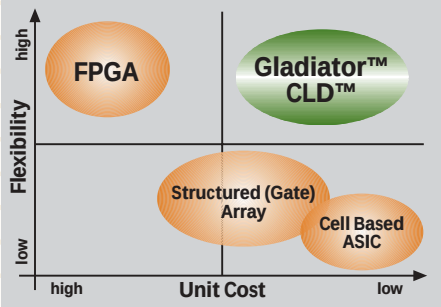
An attempt but no solution

Recently, Structured Arrays have been introduced in an attempt to address the shortcomings of standard cell ASICs. These devices look and work much like the well known gate arrays, using multiple metal layers for configuration, but do not offer a viable alternative. Structured Arrays mandate a gate array style design flow where the user passes the netlist or RTL to the ASIC vendor for timing closure and back end design, resulting in potentially lengthy timing closure cycles. Some of the proposed devices include embedded processors or other hardwired functions, but all fall short of providing FPGA-like flexibility.

Gladiator CLD – The Solution

Low Cost, High Performance, Rapid Time-to-Market, Field-Upgradeable

Gladiator CLD is a family of configurable logic devices combining the benefits of FPGAs and ASICs in a low-cost, yet versatile device. These benefits are achieved by using a combination of Leopard Logic's proprietary HyperBlox™ FP and MP fabrics, along with dedicated memories and Multiply-Accumulate (MAC) units. With a design cycle and an upfront investment comparable to an FPGA, Gladiator CLD delivers the performance and capacity of an ASIC at a very attractive price point. This results in the lowest Total Cost of Ownership (TCO) for products with unit volumes ranging from 1k to 100k units.



The performance and ease-of use of Gladiator CLD enables customers to instantly tap a vast array of existing Intellectual Property (IP) components from prior designs or third parties. Leopard Logic is teaming up with leading IP providers to assure efficient access to best-in-class, silicon proven IP solutions for its target applications.

Gladiator CLD Benefits

- Meets cost, power, performance and flexibility requirements
- Fast turn-around time accelerates time to revenue
- Lower Total Cost of Ownership than ASICs and FPGAs
- Low risk solution with minimum NRE
- Quick timing closure at customer site
- IP protected in a traceable device

"The current approach to future proof system designs is to combine FPGAs with off-the-shelf components and ASICs. Merging ASICs with FPGAs into a single device eliminates the need for separate glue devices and can extend a products lifetime and market reach, while offering the best trade-off in terms of cost, performance and time to market."

Warren Miller,
VP of Marketing, Avnet Cilicon

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- 2-4x Higher performance than FPGA
- 10x Lower unit cost than FPGA
- 10x Lower NRE than ASIC
- Lowest TCO for 1k-100k units

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