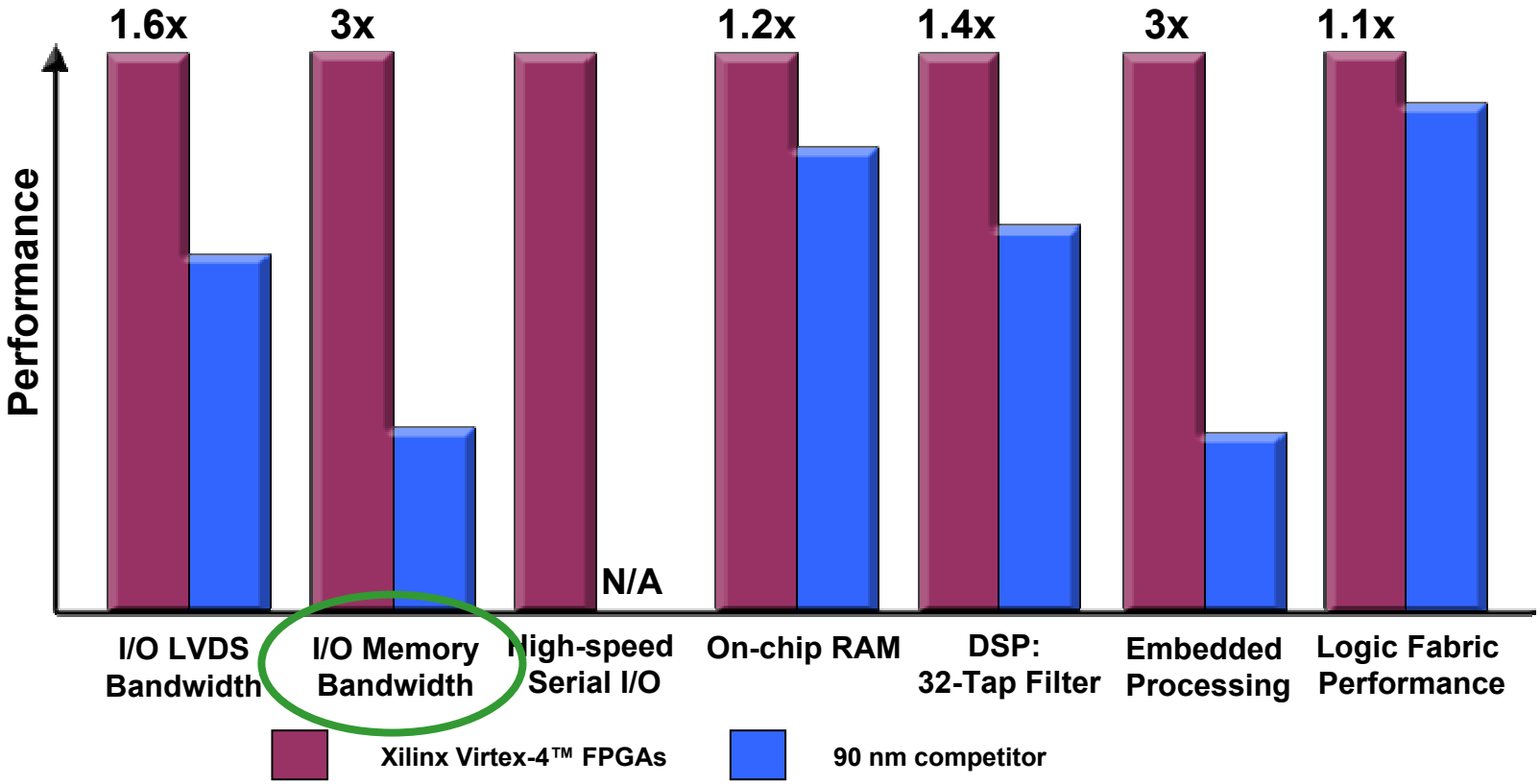
Virtex™-4 Memory Interface Advantage

High-Performance
Memory Interfaces
Made Easy

Key Messages

- High-speed memory interface design presents many challenges
- Xilinx solutions simplify physical design
  - Save time
  - Save money
  - Achieve highest bandwidth
  - Faster time to market

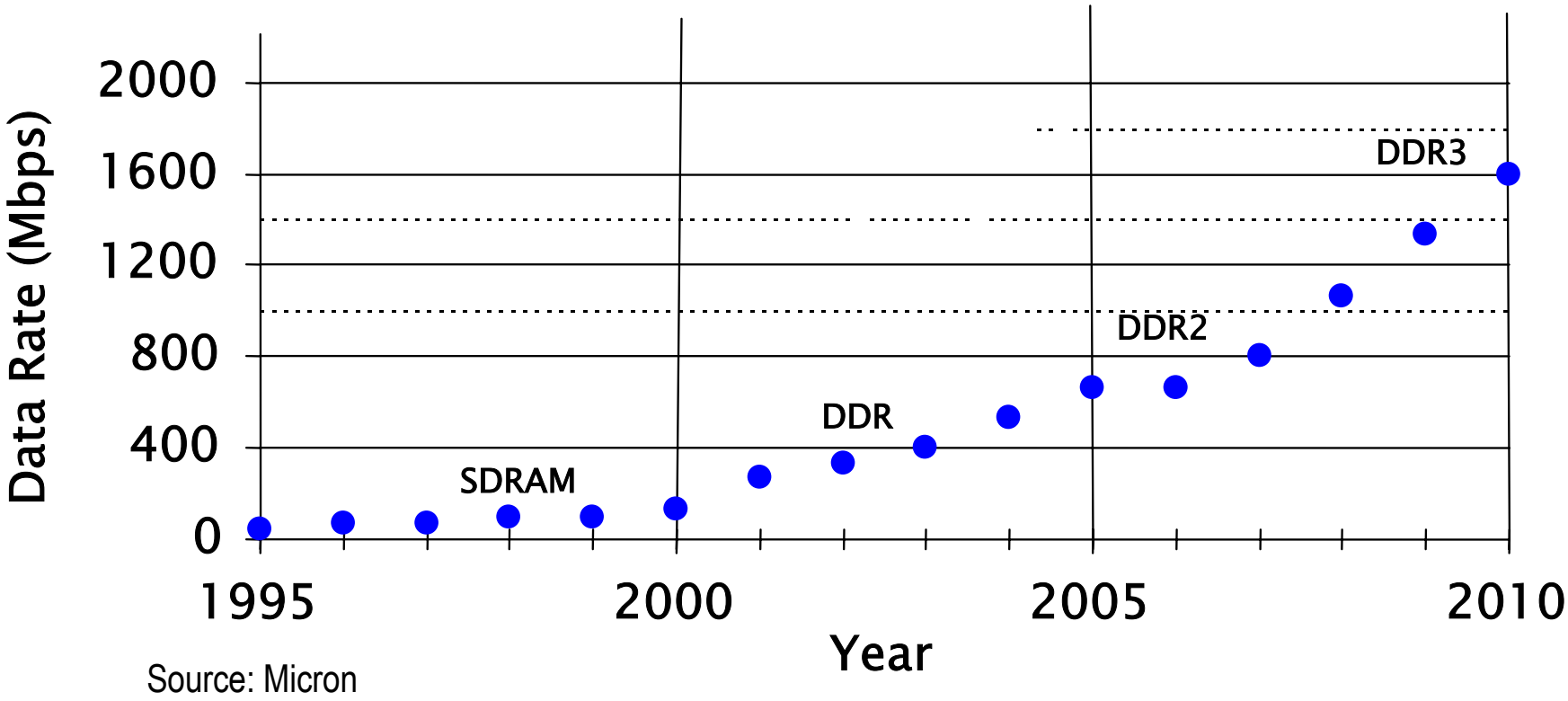
Virtex-4 Leads in 7 of 7 Performance Criteria



Data based on competitor's published datasheet numbers

Performance up to 3x higher than competing FPGAs

Mainstream Memory Data Rates

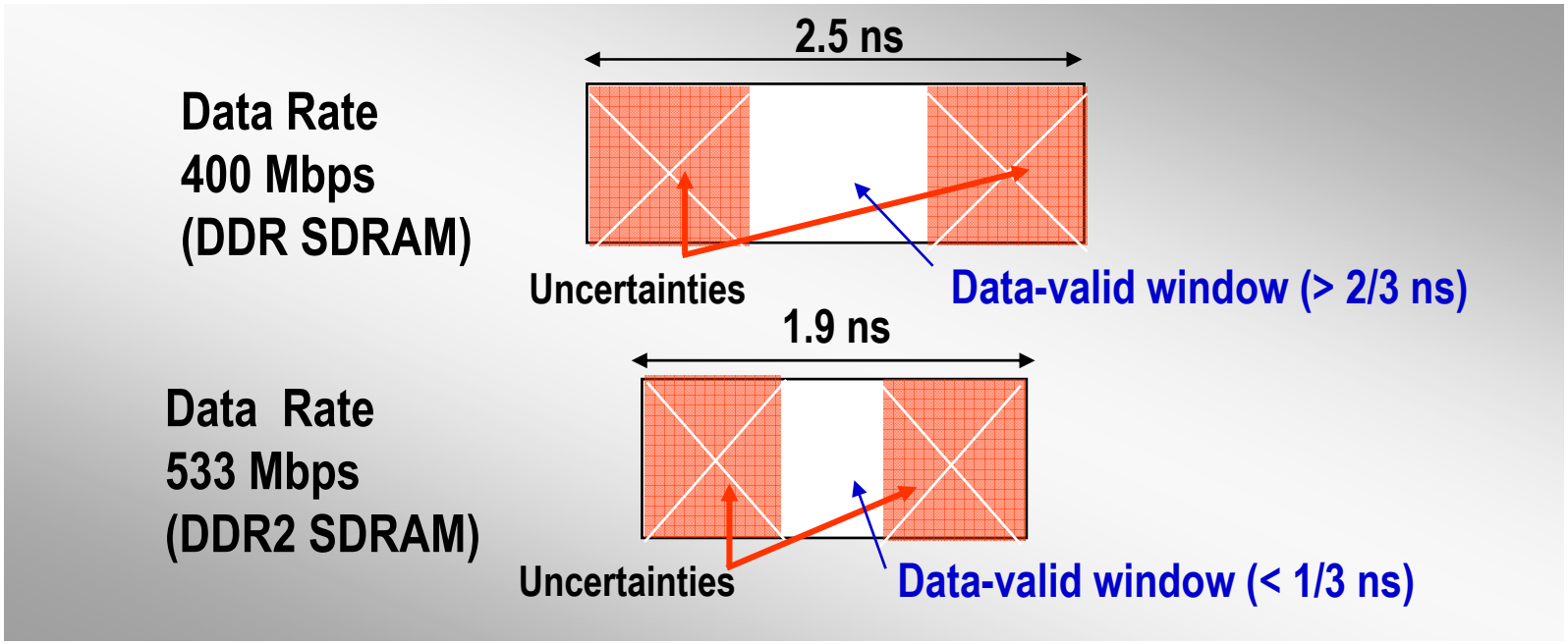


Source: Micron

Mainstream memory data rates doubling every four years

Shrinking Timing Margins

- Data-valid window shrinks faster than clock period
  - Faster data rates but similar device and system uncertainties



Interface timing becomes more demanding

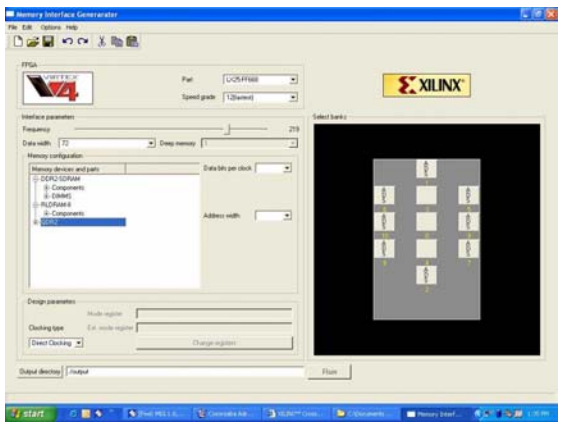
Memory Interface Design Challenges

1. Timing-critical physical layer
   - Read-data capture
   - Meeting the timing budget with reliable design margins
2. High bandwidth system requirements
   - Data Rate x Bus Width
   - Resolving signal integrity issues
   - Meeting I/O placements and board routing requirements
3. Complex memory controller design

Based on more than 300 customer surveys

Xilinx Makes it Easy

- Virtex-4 FPGA built-in silicon features
  - Chipsync™ in every I/O
- Hardware-verified designs for highest performance interfaces
  - DDR2 SDRAM, DDR SDRAM, QDR II SRAM, RLDRAM II
- Memory Interface Generator (MIG)
  - Generates your custom memory controller and physical layer interface in minutes using hardware verified designs

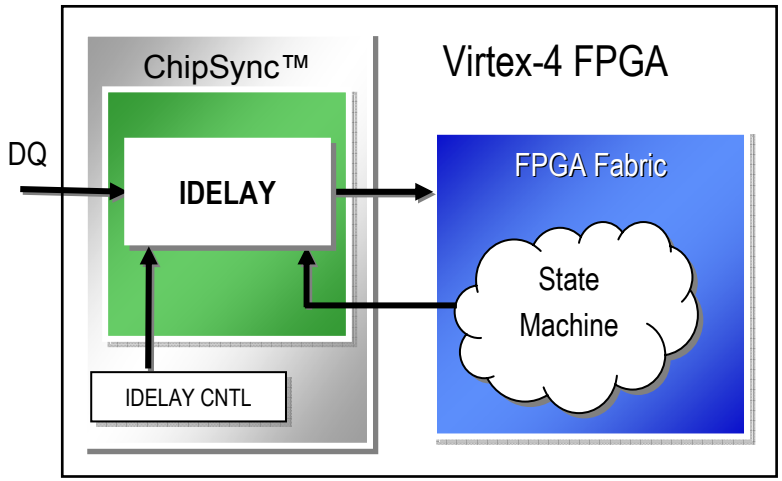


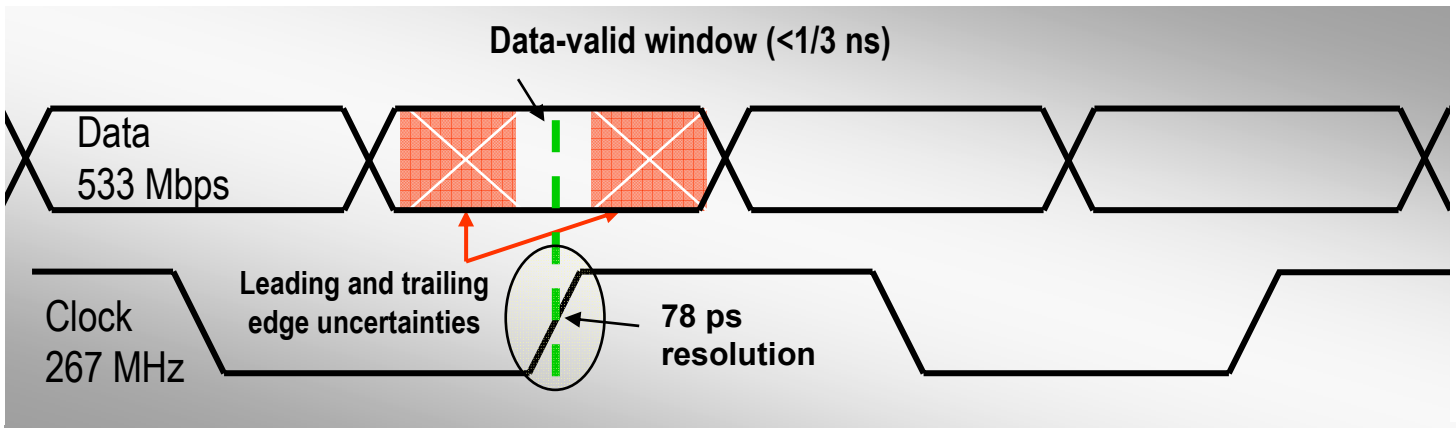
Memory Interface Generator

ML461- Development System

Precise Data-to-Clock Centering

- Unique Virtex-4 FPGA solution with ChipSync IDELAY
  - "Run time" centering of data-to-clock
  - 64 tap delays with 78 ps resolution
  - Maximizing design margins for higher system reliability





Not available in any other FPGA, ASIC or ASSP

Data Rate x Bus Width

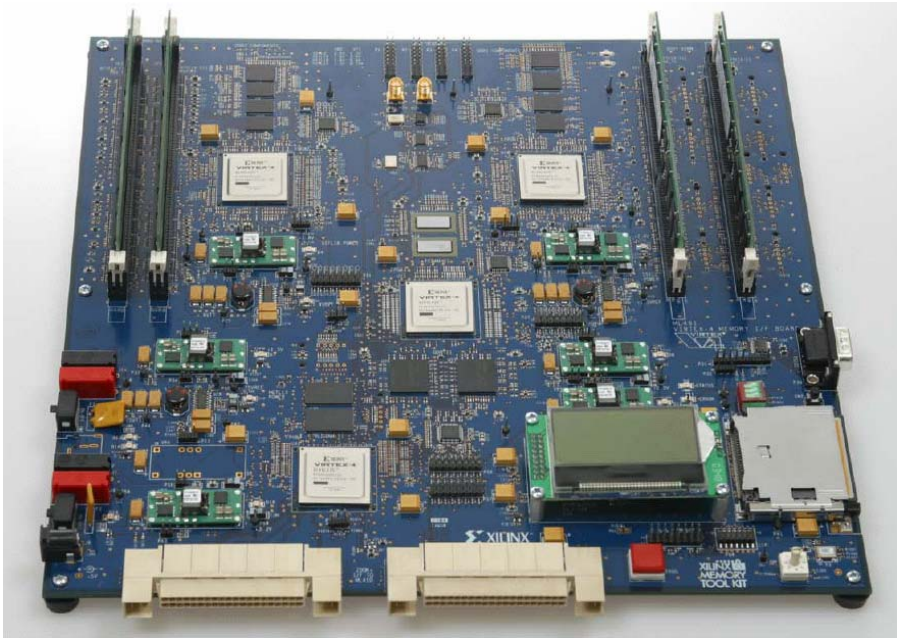
- Any I/O can be used for Data, Strobe/Clock or Address/Controls
  - Chipsync built in every I/O
  - Any Data to Strobe ratio from x4 to x36 is supported
- Data rates of 600 Mbps for single-ended I/O standards
- Up to 259 Gbps data bandwidth using 432 Data bits
  - Superior SSO performance with innovative package design

Device	Pkg	Max Data
LX25, LX40, LX60	FF668	144
LX40, LX60	FF1148	288
LX80, LX100, LX160	FF1148	360
LX100, LX160, LX200	FF1513	432

3 x higher bandwidth than competing solutions

Multiple Designs Simulated and Verified in Hardware

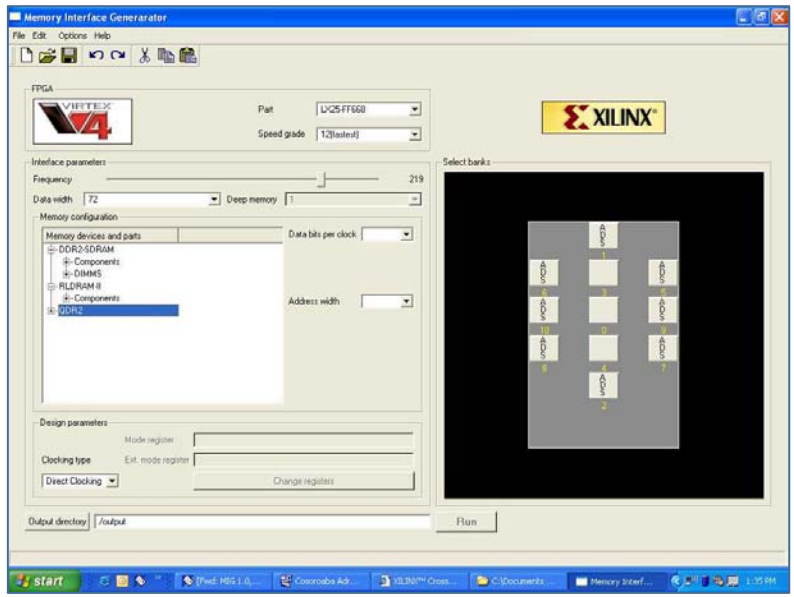
- ML461 Development System
  - 4 x LX25 devices supporting multiple memory interfaces
  - JTAG interface for ChipScope Pro (in circuit logic analyzer)
  - Reference designs verified on it
- Available now
  www.xilinx.com/ml461



	DDR2	DDR	QDR II	RLDRAM II	FCRAM II
Data rate	533 Mbps	400 Mbps	1.2 Gbps	600 Mbps	600 Mbps
CLK Rate	267 MHz	200 MHz	300 MHz	300 MHz	300 MHz
Data Width	144 bit (DIMM)	144 bit (DIMM)	(72+72) bit	36 bit	36 bit

Memory Interface Generator Makes Design Easy

- Generates :
  - HDL code
  - Constraints file
  - Synthesizable test bench
- Download now: FREE
  www.xilinx.com/memory



User-friendly GUI

Design your controller with complete flexibility

Xilinx Solves Memory Interface Design Challenges

- Timing critical physical layer
  - Chipsync built in every I/O
    - Clock-to-data centering at “run time”
- High bandwidth system requirements
  - Column-based architecture and superior packaging
  - 600Mbps x 432 bit wide buses
- Complex memory controller design
  - Hardware verified solutions for all popular memory types (DDR2, DDR SDRAM, QDR II SRAM, RLDRAM II)
  - Memory Interface Generator (MIG)
    - Generates your design in minutes

Memory Interfaces Made Easy

How to Get Started

- Leverage complete hardware-verified solutions to ensure first-time design success
- Get the latest Virtex-4 memory design solutions on www.xilinx.com/memory
  - Memory Interface Generator (MIG)
  - Application Notes
  - ML461 - Advanced Memory Development System
    - Board level solution: reference designs, schematic & gerber files
    - DDR2, DDR SDRAM, QDR II SRAM,RLDRAM II, FCRAM II
- Arrange for an on-site demo

Accelerate Your Design Cycle