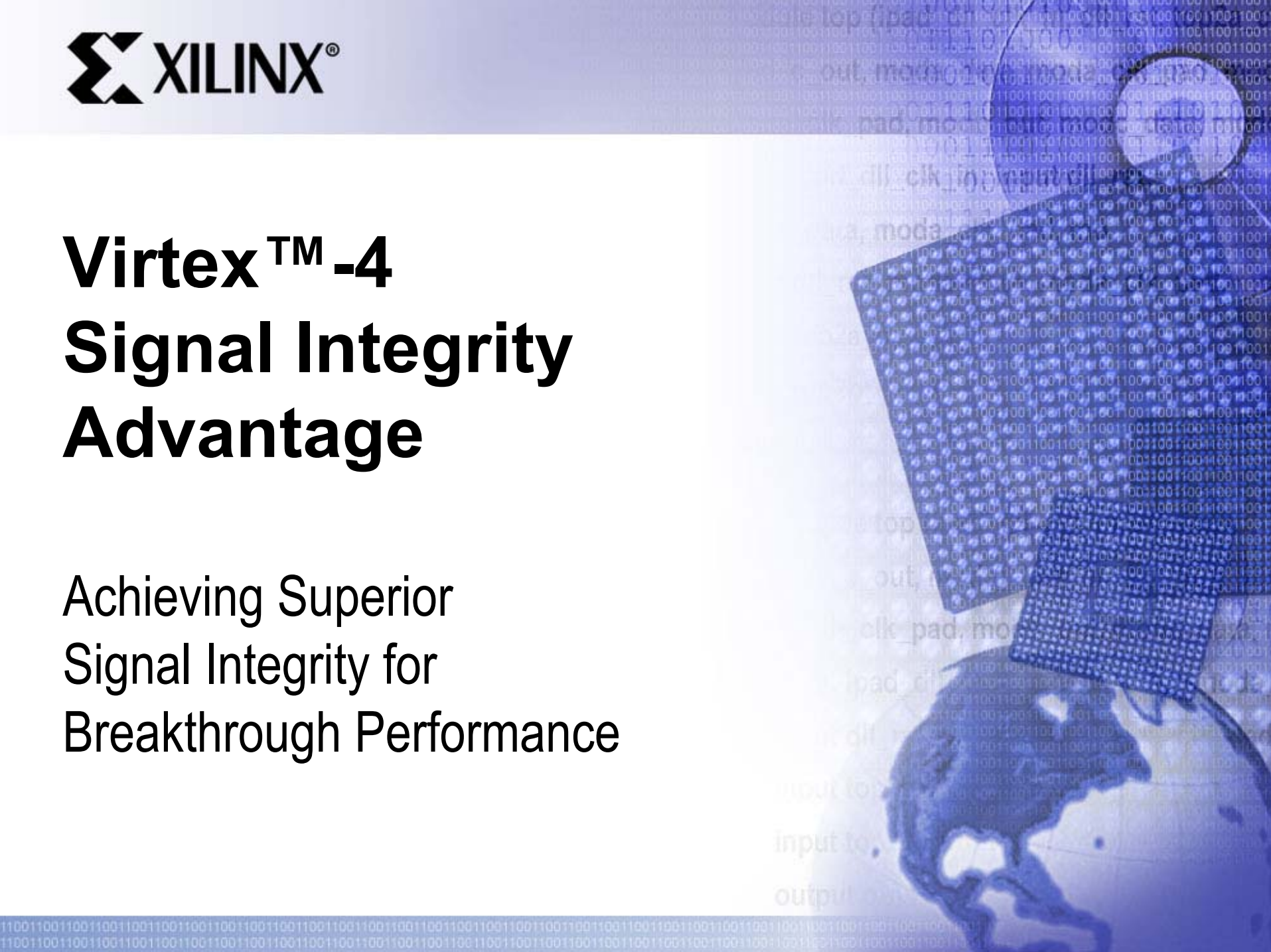
Virtex™-4 Signal Integrity Advantage

Achieving Superior
Signal Integrity for
Breakthrough Performance



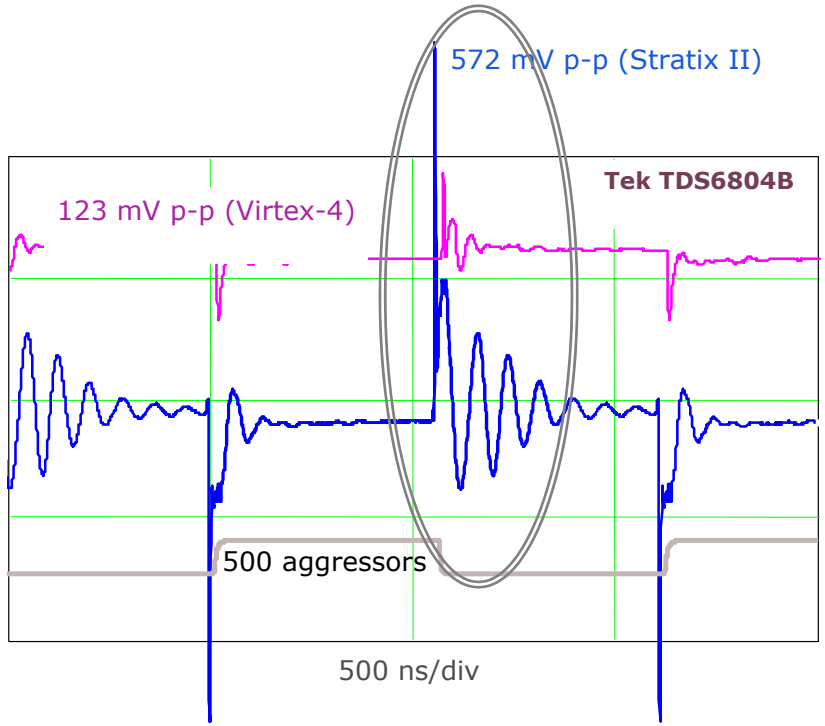
Key Messages

- Noise can kill your wide parallel interface (>32 bits)
- New Virtex-4 with SparseChevron™ package exhibits 4x to 7x lower measured noise in comparison to competition
- Industry expert validates Xilinx package design
- Benefits engineers designing single-ended parallel interfaces (e.g. Memory Interfaces)

Achieving Superior Signal Integrity For Breakthrough Performance

Listen to On-demand Seminar Archive

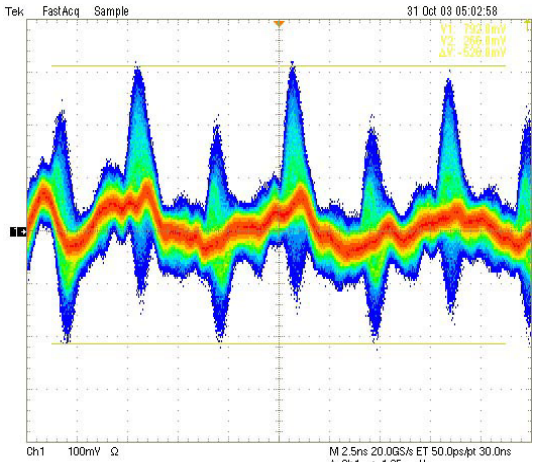
BGA Crosstalk
By
Dr. Howard Johnson
www.xilinx.com/virtex4/si



4X – 7X Lower Noise than Competition

Introduction

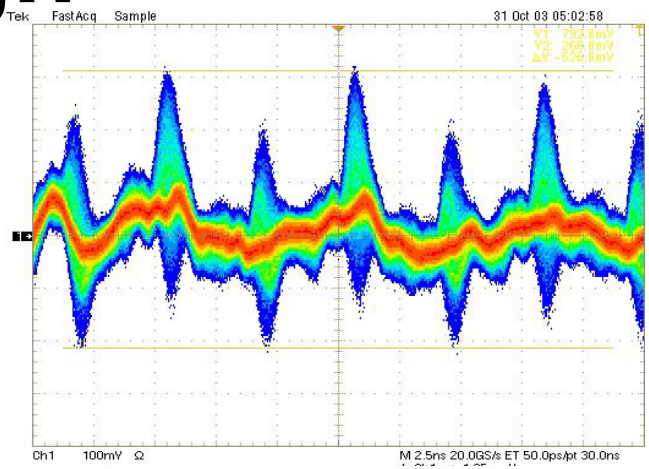
- Signal Integrity affects System Performance
- Wide, single-ended interfaces
  - DDR, QDR memory interfaces
  - Faster bit rates, Faster edge rates
- Faster is better, but…
  - Noise becomes a big concern
  - Simultaneously switching output noise (SSN)
  - More jitter + reduced timing margin = potential system failure



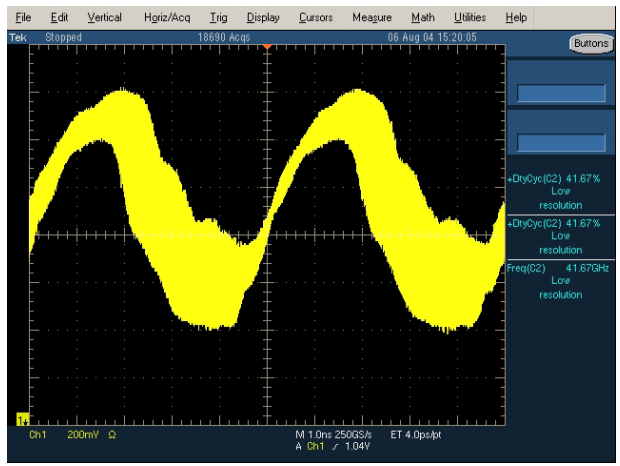
Packaging Impacts System Design

Pin-out & Packaging

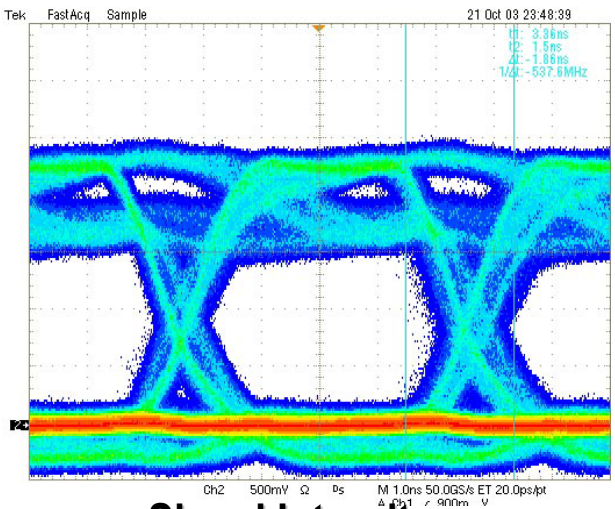
Package and PCB Inductance and Crosstalk



Ground Bounce/Voltage Collapse



System Jitter



Signal Integrity

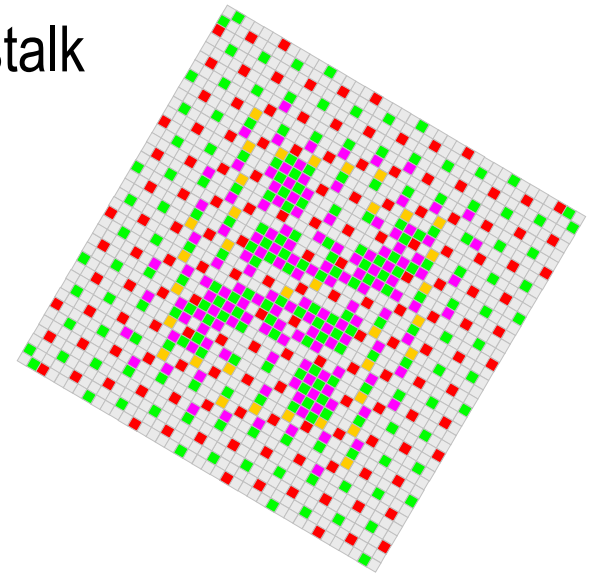
Package Design is Critical

- Choosing the right package is essential for controlling system noise
  - Possible workarounds for board design issues
  - Almost no control over package problems
- Package-related noise problems difficult to debug and solve
  - Lost Time, Money, Market Window

Need a Well-Designed, Low-Inductance Package!

Virtex-4 Provides Advanced Packaging Solutions

- Improved signal, power integrity and crosstalk
  - Minimizes package & PCB inductances
  - More usable I/Os than competing solution
- Designed & verified with extensive simulation and hardware testing
- No additional PCB costs to customers
  - Use same number of PCB layers as previous generations

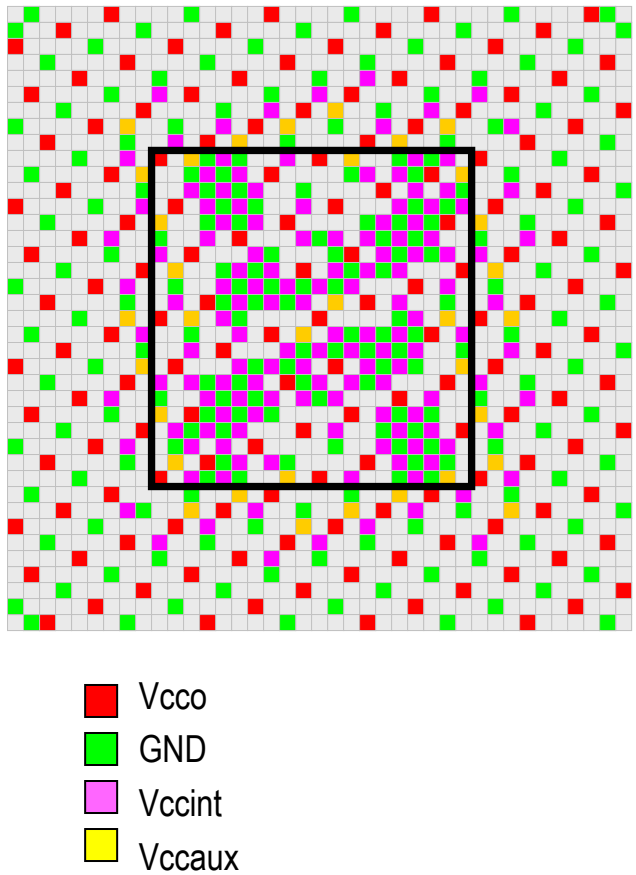


The Best Approach for High Pin-Count 90nm FPGAs

Virtex-4 SparseChevron™ Package

- Superior pinout architecture
  - Excellent signal-to-VCC/GND-pin ratio
  - Every signal pin adjacent to VCC/GND ball
- High-frequency on-package decoupling capacitors
- Continuous Power/Gnd planes

FF1513 SparseChevron Pinout

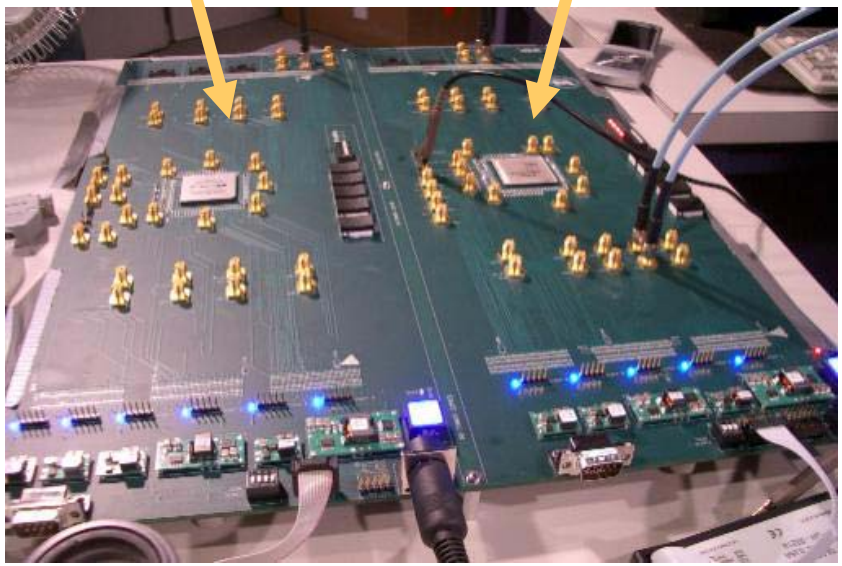


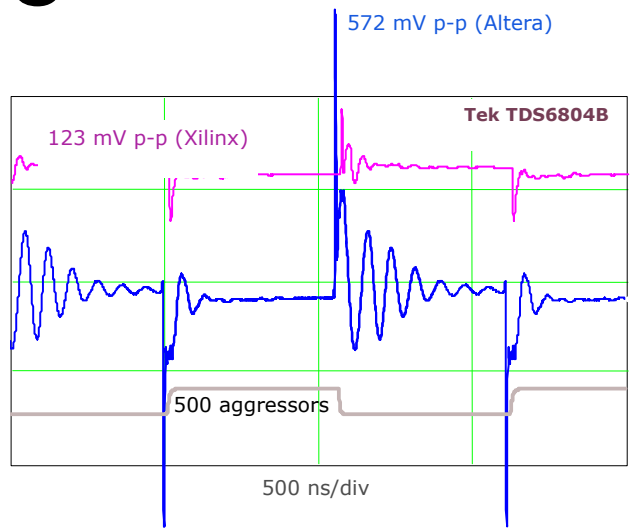
FPGA Industry Best Noise Performance

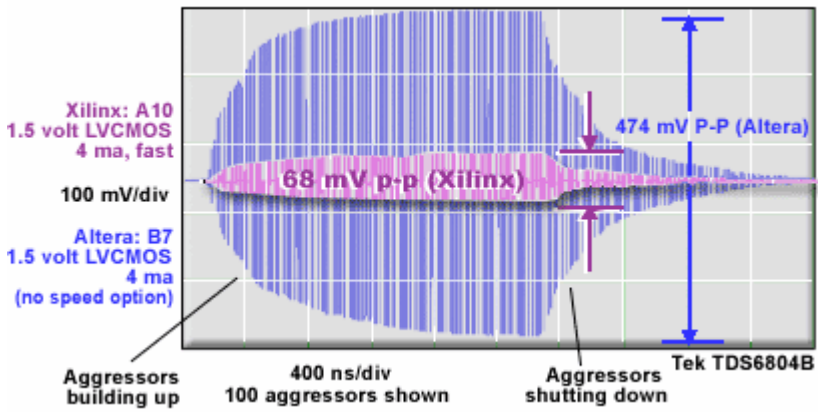
4X-7X lower measured noise in side-by-side comparison

Altera Stratix II
2S60
F1020 pkg.
32x32 BGA

Xilinx Virtex-4
LX60
FF1148 pkg.
34x34 BGA







Summary

- Successful high-speed system design requires attention to signal integrity
- Good package design is critical
- Virtex-4 with SparseChevron package exhibits 4X-7X lower noise than competition
- Validated by industry expert
  - Read Dr. Howard Johnson's report and view on-demand seminar
    www.xilinx.com/virtex4