

VGA Interface

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Contents

1.0 About this design.....	1
2.0 Files needed for this design.....	1
List of Files.....	1
File Descriptions	1
3.0 Description of the design.....	2
Synchronisation.....	2
Resolution / Refresh Rates	2
Colour Map.....	2
High Colour.....	3
Test Pattern.....	3
4.0 Extensions and Notes	3

1.0 About this design

The VGA Interface is designed to be a simple interface to a VGA monitor using the RAMDAC included on the XSV board. It contains support for a 256 colour programmable colour map and high colour (15 bit) displays. The current resolution and refresh rate is set to 800x600 @ 72Hz with a 50MHz clock and is easily changeable.

2.0 Files needed for this design

List of Files

- prgramdac.vhd
- hicolvga.vhd
- vga.vhd
- vgacore.vhd
- vgapins.ucf

File Descriptions

prgramdac.vhd

Programs the RAMDAC for use in either high colour or 256 colour mode.

hicolvga.vhd

Default top level file which displays a pretty programmable cross-hatched pattern on the monitor in 15-bit colour.

vga.vhd

Alternative top level for the project. Displays all 256 colours programmed in the RAMDAC as a test pattern. The RAMDAC programmer must have some comments changed to use this.

vgacore.vhd

Controls the synchronisation timings (hsync and vsync) to the monitor.

highcolpins.ucf

Constraints file for the high colour version of the design.

vgapins.ucf

Constraints file for the pseudo colour version of the design.

3.0 Description of the design

Synchronisation

The hsync and vsync lines (horizontal sync and vertical sync) are controlled in `vgacore.vhd`. Vsync is timed off hsync overflows to simplify the timing logic for vsync. The timings for these affect the resolution and refresh rate of the monitor, and are set up as generics and constants so they can be easily changed. Note that incorrect settings of these will result in aberrations in the picture, or no picture being displayed at all.

Resolution / Refresh Rates

Sample VESA standard timings can be found at <http://www.angelfire.com/nt/sucks/XF86Config.txt> (at the end of the text file), and a list of the timings and clock speeds that some (older) monitors and video cards use can be found at <http://www.zomby.net/hardware/sog/modeDB.txt>. These provide the horizontal timings (counted off the given clock) and vertical timings (as off the overflows of hsync) required for each resolution and refresh rate. Note that the exact clock frequency is not needed (it is fine for 640x480 to run off a 25MHz clock, rather than the 25.175MHz clock specified). Other user resolution and refresh rates can be created via trial and error (or some common sense).

Colour Map

One of the options of the RAMDAC is to produce colours via a programmable 256 colour lookup table, also known as a colour map (this is pseudo colour mode). Before operation, the colour map must be

programmed with sets of three byte colour values (one byte for red, one byte for green and one byte for blue). To produce a certain stored colour, the location of the data in the colour map is asserted on the pixel bus to the RAMDAC. To switch between using a colour map or high colour, comment and uncomment the required lines (see the comments) in the prgramdac.vhd file. It is possible to use custom colour maps, or to use one of the ones provided by uncommenting the desired lines.

High Colour

High colour can produce a possible 32,768 colours by sending two bytes of data to the RAMDAC using 15 bit data, with 5 bits for each primary colour (the MSbit sent is ignored). Sending two bytes of data on the pixel lines means that the routine that sends the data to the RAMDAC must now be double clocked, so both the bytes of data are sent in one (50MHz) clock cycle. This can be seen in the high colour version of the vga file. An alternative is to use the single edge mode of this input style, send the bytes on separate clock cycles and produce an effective resolution of 400 * 600 pixels. This mode is used in the video input project.

Test Pattern

During operation, each of the different VGA top level files will produce a rotatable test pattern. For more information on how to change the display see the comments in the files. Here are the switches that the inputs are mapped to. The easiest way to work out what they do is experiment, so have fun.

Pseudo Colour:

DIP 1: Control whether the test pattern rotates
DIP 2: Control direction of rotation
DIP 3: Control whether test pattern is horizontal or vertical

High Colour:

DIP 1-2: Control red component contribution of test pattern
DIP 3-4: Control green component contribution of test pattern
DIP 5-6: Control blue component contribution of test pattern
DIP 7: Control whether the test pattern rotates horizontally
DIP 8: Control whether the test pattern rotates vertically
PB 1: Control direction of horizontal rotation
PB 2: Control direction of vertical rotation

4.0 Extensions and Notes

There are several extensions and fixes which could be done to this project. The display created on the monitor isn't clear – it has a slight horizontal shimmer, and the reason for this isn't apparent as changing the timings, resolution and refresh rate doesn't remove it. Perhaps playing with the constraints could lessen or remove this. Other things which can be done is adding support for different resolutions and refresh rates.

Several things must be noted about the design. The high colour project must be implemented with a high effort otherwise glitching will occur due to the additions when displaying the patterns thanks to the double edge clocking. Also, the RAMDAC programming lines are shared with some outputs of the PHY device, so the

outputs must be disabled by lowering the `trste` (tristate) input to the PHY. Interfacing the device to show pictures on a VGA monitor is as easy as setting the pixel data lines at the correct time according to the values of `vloc` and `hloc` in `vga.vhd`.