Table B--Embedded logic analyzers

Company	Product	Supported architectures and devices	Maximum number of channels	Maximum sampling rate	Maximum per-channel sampling depth	Number of triggers	Other features	Price
Actel	Silicon Explorer II	All Actel antifuse devices — eX, MX, SX, SX-A	18	100 MHz synchronous	64K per channel	4 levels of triggering	Serial port connection, dynamic access into internal nodes	$1,495
Actel	Silicon Explorer II Lite	All Actel antifuse devices — eX, MX, SX, SX-A	NA	100 MHz synchronous	64K per channel	4 levels of triggering	Serial port connection, dynamic access into internal nodes	$499
Altera	SignalTap Embedded Logic Analyzer	Altera Stratix, APEX II, APEX 20K, APEX 20KE, APEX 20KC, Mercury	Limited only by PLD device resources	Users specify acquisition clocks from their PLD design, maximum sampling rate is limited only by the target PLD device architecture and the speed of users clock in the design	Up to 128K samples per channel dependent on device targeted, captured data can be routed to external pins for larger sample depth requirements	Limited only by PLD device resources	Captures state of any internal node or I/O pin in an Altera PLD at system speeds. No changes to design files are required. Supports inserting multiple analyzers in a single PLD device and logging captured data.	Included as part of the Quartus II design software. An annual subscription for the Altera design software (including Quartus II) is $2,000 for a node-locked PC license
FS2	ISA-Eclipse, ISA-Eclipse/T (off-chip trace)	QuickLogic Eclipse	1 to 4 sets of 32 channels per set	100MHz synchronous (clock supplied by fabric)	4k frames with on-chip trace buffer; 128K frames with off-chip trace buffer (/T versions)	Up to 2 triggers for on-chip CLAM + 2 sequence states, 4 triggers for off-chip CLAM + 4 sequence states	MIPS EJTAG run control with Green Hills MULTI, Accelerated Technology codelab debug support, CLAM interface software, Verilog/VHDL source code for CLAM logic	$1995 (ISA-Eclipse), $3995 (ISA-Eclipse/T)

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Triscend	Embedded JTAG-based emulator/debugger	Triscend E5	Probe any logic cell output or flip-flop output, monitor or control any memory-mapped location	40 MHz	Samples stored on PC	Two hardware breakpoints triggered on various bus transaction types, breakpoint triggers available from programmable logic, software breakpoint instruction	Start/stop embedded 8051, set internal hardware and software breakpoints, capture target snapshots, single-stepping, IEEE 1149.1 JTAG interface	Included on-chip
Triscend	Embedded JTAG-based emulator/debugger	Triscend A7	Probe any logic cell output or flip-flop output, monitor or control any memory-mapped location	60 MHz	Samples stored on PC	Two hardware breakpoints triggered on various bus transaction types, breakpoint triggers available from programmable logic	Start/stop embedded 8051, set internal hardware and software breakpoints, set tracepoints, capture target snapshots, single-stepping, 512-transaction trace buffer, IEEE 1149.1 JTAG interface	Included

NA=not applicable